

RM67295 Datasheet

Single Chip Driver with 16.7M color
for 1080RGBx1920 OLED driver

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Date : Aug. 18, 2016

Revision History

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0.0	2016/08/18	Initial	

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1. General Description

The RM67295 device is a single chip solution for LTPS AMOLED that incorporates gate drivers and is capable of 1080RGBx1920 operation. It utilizes SPR (sub pixel rendering) algorithm to reduce pixel size while keeping the same picture quality. It is a RAM-less IC. A timing controller with glass interface level-shifters and a glass power supply circuit.

The RM67295 supports MIPI Interface and serial peripheral interfaces (SPI).

The RM67295 is also able to make gamma correction settings separately for RGB dots to allow benign adjustments according to panel characteristics, resulting in higher display qualities. A deep standby mode is also supported for high power saving.

This LSI is very suitable for small and medium-sized portable mobile solutions requiring long-term driving capabilities especially for cellular phone application.

2. Features

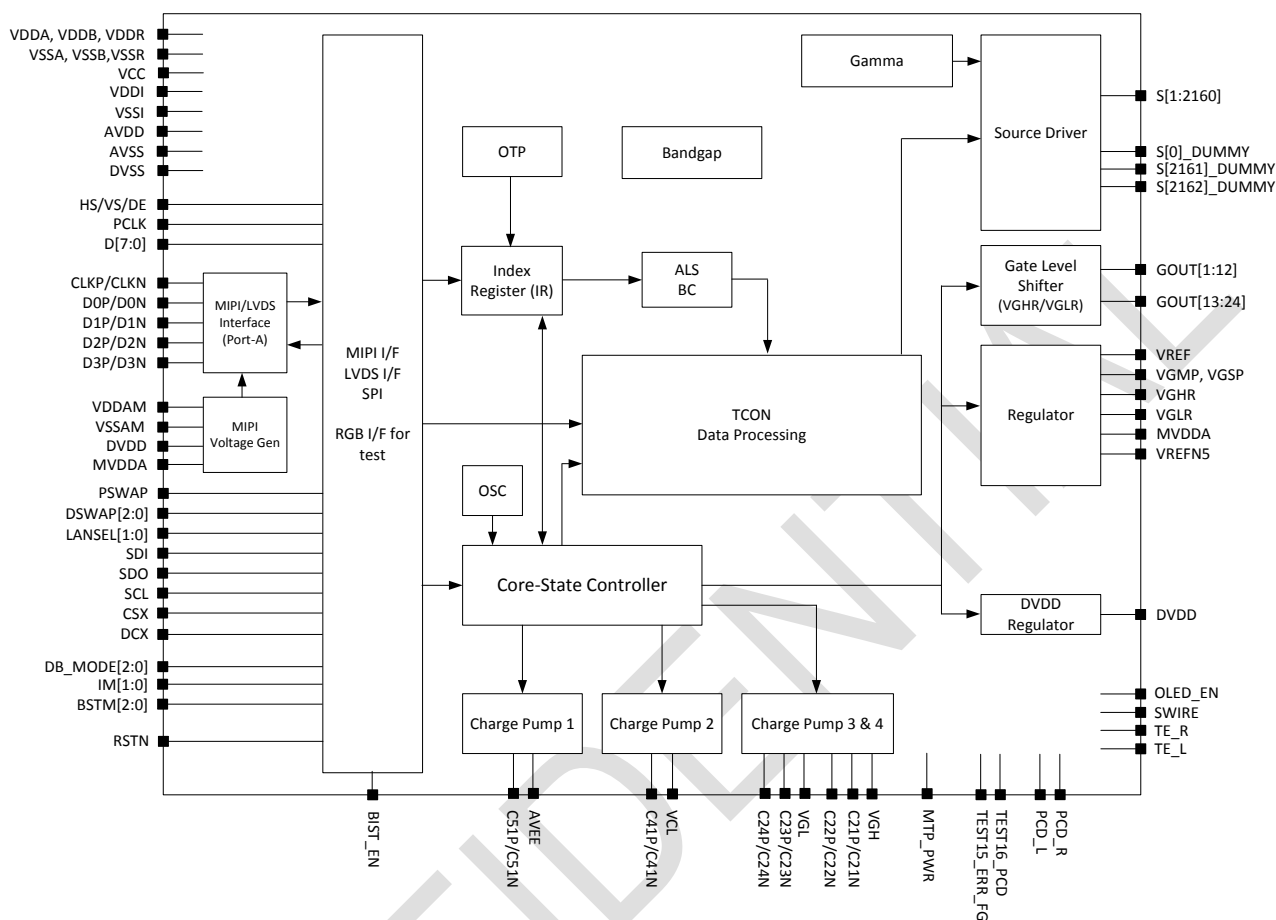
- Single chip RAM-less FHD AMOLED controller/driver
- Display resolution option
 - FHD SPR (1080x 2x 1920)
 - HD Real (720x 3x 1280)
- Display mode (Color mode)
 - Full color mode: 16.7M-colors (24-bit)
 - Reduce color mode: 262K colors (18-bit)
 - Reduce color mode: 65K colors (16-bit)
 - Idle mode: 8-colors
- Interface
 - 3-wire/4-wire SPI
 - MIPI Display Serial Interface, Support 2/3/4 data lanes (max data rate is 1Gbps/lane)
- Abundant color display and drawing functions
 - Programmable gamma correction function for 16.7 million color display
 - Individual gamma correction setting for RGB dots
- Color Enhancement
 - Local Saturation Adjustment
 - Sharpness/Skin Tone/Local Hue Adjustment
- Rendering IP
 - Support FHD Rendering Function
 - Support RGB delta and RGBG types
- Power Saving Mode
 - Auto Current Limitation (ACL)
 - Ambient Light Sensor (ALS)

- Peripheral Control Timing and Power Generator
 - Internal oscillator
 - 2160ch outputs
 - Support programmable GOA control
 - Internal Pump for AVEE/VCL/VGH/VGL
 - Support 8-bit DAC output
 - Support S-wire interface for power IC control
- Miscellaneous Function
 - Built-in OTP (MTP) for adjusting gamma, timing, and etc.
- Operating Condition
 - VDDI: 1.65V~ 3.6V (for Regulator Power Source/Interface Power)
 - VDDA/VDDDB/VDDR: 2.5V~ 3.6V (for Analog Power Supply)
 - VCC/VDDAM: 1.65V~ 3.6V (for DVDD/MVDDA Regulator)
 - AVDD: 4.5V~ 6.5V
 - Operating temperature: -40~85°C
 - Storage temperature: -55~ 125°C
- Package: COG

■ Power Supply Specification

No.	Item		Description
1	Source Driver		2160 pins
2	Gate control timing Level shift		VGHR – VGLR
3	Input Voltage	VDDI	1.65V ~ 3.3V
		VDD (VDDA/VDDDB/VDDR)	2.5V ~ 3.6V
		VCC	Connect to VDDI
		VDDAM	Connect to VDDI
		AVDD	4.5V ~ 6.5V
4	OLED drive voltages	VGHR	3.5V ~ 12V (Step= 0.1V)
		VGLR	-3.5V ~ -12V (Step= -0.1V)
		VREFN5	-0.2V ~ -6V (Step= -0.1V)
5	Internal step-up circuits	AVEE	AVDD x (-1)
		VGH	AVDD + VDD, AVDD x 2 AVDD x 2+ VDD, AVDD x 3
		VGL	AVEE – AVDD, AVEE x 2 – VDD AVEE x 2 – AVDD
		VCL	VDD x (-1)

3. Block Diagram



4. Pin Description

4.1 Power Supply Pins

Signal	I/O	Function
VDDA	P	Power supply for Analog circuit VDDA, VDDDB and VDDDR should be the same input voltage level
VDDDB	P	Power supply for DC/DC converter VDDA, VDDDB and VDDDR should be the same input voltage level
VDDDR	P	Power supply for Regulator system VDDA, VDDDB and VDDDR should be the same input voltage level
VDDAM	P	Power supply for MIPI analog regulator system
VDDI	P	Power supply for interface system except MIPI interface
VCC	P	Power supply for DVDD regulator VCC can be connected to VDDI or VDD (VDDA/VDDDB/VDDDR)
AVDD	P	Power supply for Analog system
VSSA	P	System ground for Analog circuit
VSSB	P	System ground for DC/DC converter
VSSR	P	System ground for regulator system
VSSAM	P	System ground for MIPI circuit
VSSI	P	System ground for I/O circuit
DVSS	P	System ground for internal digital system
AVSS	P	System ground for source OP system.
MTP_PWR	P	MTP programming power supply pin (8V typical) Must be left open or connected to DVSS in normal condition.

4.2 Interface Pins

Signal	I/O	Function
CSX	I	Chip select input pin ("Low" enable) in 80-series MPU I/F and SPI I/F. This pin is not used for MIPI I/F, please connect to VSSl.
SCL	I	SCL: Synchronous clock signal in SPI I/F. This pin is not used for MIPI I/F, please connect to VSSl.
DCX	I	Display data / command selection in 8-bit SPI I/F. DCX = "0" : Command DCX = "1" : Display data or Parameter This pin is not used for 9-bit/16-bit SPI or MIPI I/F, please connect to VSSl.
SDI	I/O	SDI: serial input signals in SPI I/F. The data is input on the rising/falling edge of the SCL signal. This pin is not used for MIPI I/F, please connect to VSSl.
SDO	O	Serial output signal in SPI I/F. The data is output on the rising/falling edge of the SCL signal. If the host places the SDI line into high-impedance state during the read interval, the SDI and SDO can be tied together. This pin is not used for MIPI I/F, please open it.

4.3 MIPI Interface Pins

Signal	I/O	Function																								
HSSI_CLK_P HSSI_CLK_N	I	-These pins are DSI-CLK+/- differential clock signals if MIPI interface is used. -HSSI_CLK_P/N are differential small amplitude signals. Ensure the trace length is shortest so that the COG resistance is less than 10 ohm. -If not used, please connect these pins to VSSAM.																								
HSSI_D0_P HSSI_D0_N	I/O	-These pins are DSI-D0+/- differential data signals if MIPI interface is used. -HSSI_D0_P/N are differential small amplitude signals. Ensure the trace length is shortest so that the COG resistance is less than 10 ohm. -If not used, please connect these pins to VSSAM.																								
HSSI_D1_P HSSI_D1_N	I/O	-These pins are DSI-D1+/- differential data signals if MIPI interface is used. -HSSI_D1_P/N are differential small amplitude signals. Ensure the trace length is shortest so that the COG resistance is less than 10 ohm. -If not used, please connect these pins to VSSAM.																								
HSSI_D2_P HSSI_D2_N	I/O	-These pins are differential data signals if MIPI interface is used. -HSSI_D2_P/N are differential small amplitude signals. Ensure the trace length is shortest so that the COG resistance is less than 10 ohm. -If not used, please connect these pins to VSSAM.																								
HSSI_D3_P HSSI_D3_N	I/O	-These pins are differential data signals if MIPI interface is used. -HSSI_D3_P/N are differential small amplitude signals. Ensure the trace length is shortest so that the COG resistance is less than 10 ohm. -If not used, please connect these pins to VSSAM.																								
LANSEL[1:0]	I	<div>Input pin to select number of data lanes in MIPI interface.</div> <table><tr><th>LANSEL[1]</th><th>LANSEL[0]</th><th>DATA LANE of MIPI</th></tr><tr><td>1</td><td>1</td><td>4-lane</td></tr><tr><td>1</td><td>0</td><td>3-lane</td></tr><tr><td>0</td><td>1</td><td>2-lane</td></tr></table> <div>If not used, please connect to VSSI.</div>	LANSEL[1]	LANSEL[0]	DATA LANE of MIPI	1	1	4-lane	1	0	3-lane	0	1	2-lane												
LANSEL[1]	LANSEL[0]	DATA LANE of MIPI																								
1	1	4-lane																								
1	0	3-lane																								
0	1	2-lane																								
DSWAP[2:0] PSWAP	I	<div>Input pin to select HSSI_D0/D1/D2/D3 data lane sequence and polarity in high speed interface only.</div> <div>For MIPI interface, both DSWAP and PSWAP function are available.</div> <div>If not used, please connect to VSSI.</div> <table><tr><th>PSWA P</th><th>DSWAP[2:0]</th><th>HSSI_D3_P</th><th>HSSI_D3_N</th><th>HSSI_D0_P</th><th>HSSI_D0_N</th><th>HSSI_CLK_P</th><th>HSSI_CLK_N</th><th>HSSI_D1_P</th><th>HSSI_D1_N</th><th>HSSI_D2_P</th><th>HSSI_D2_N</th></tr><tr><td>0</td><td>000</td><td>D3P</td><td>D3N</td><td>D0P</td><td>D0N</td><td>CLKP</td><td>CLKN</td><td>D1P</td><td>D1N</td><td>D2P</td><td>D2N</td></tr></table>	PSWA P	DSWAP[2:0]	HSSI_D3_P	HSSI_D3_N	HSSI_D0_P	HSSI_D0_N	HSSI_CLK_P	HSSI_CLK_N	HSSI_D1_P	HSSI_D1_N	HSSI_D2_P	HSSI_D2_N	0	000	D3P	D3N	D0P	D0N	CLKP	CLKN	D1P	D1N	D2P	D2N
PSWA P	DSWAP[2:0]	HSSI_D3_P	HSSI_D3_N	HSSI_D0_P	HSSI_D0_N	HSSI_CLK_P	HSSI_CLK_N	HSSI_D1_P	HSSI_D1_N	HSSI_D2_P	HSSI_D2_N															
0	000	D3P	D3N	D0P	D0N	CLKP	CLKN	D1P	D1N	D2P	D2N															

		001	D3P	D3N	D2P	D2N	CLKP	CLKN	D1P	D1N	D0P	D0N
		010	D2P	D2N	D1P	D1N	CLKP	CLKN	D0P	D0N	D3P	D3N
		011	D0P	D0N	D1P	D1N	CLKP	CLKN	D2P	D2N	D3P	D3N
		100	D3P	D3N	D1P	D1N	CLKP	CLKN	D0P	D0N	D2P	D2N
		101	D3P	D3N	D1P	D1N	CLKP	CLKN	D2P	D2N	D0P	D0N
		110	D2P	D2N	D0P	D0N	CLKP	CLKN	D1P	D1N	D3P	D3N
		111	D0P	D0N	D2P	D2N	CLKP	CLKN	D1P	D1N	D3P	D3N
	1	000	D3N	D3P	D0N	D0P	CLKN	CLKP	D1N	D1P	D2N	D2P
		001	D3N	D3P	D2N	D2P	CLKN	CLKP	D1N	D1P	D0N	D0P
		010	D2N	D2P	D1N	D1P	CLKN	CLKP	D0N	D0P	D3N	D3P
		011	D0N	D0P	D1N	D1P	CLKN	CLKP	D2N	D2P	D3N	D3P
		100	D3N	D3P	D1N	D1P	CLKN	CLKP	D0N	D0P	D2N	D2P
		101	D3N	D3P	D1N	D1P	CLKN	CLKP	D2N	D2P	D0N	D0P
110		D2N	D2P	D0N	D0P	CLKN	CLKP	D1N	D1P	D3N	D3P	
111		D0N	D0P	D2N	D2P	CLKN	CLKP	D1N	D1P	D3N	D3P	
Note: For MIPI 3-Lane case (LANSEL[1:0]= 10), the D3P/N are not active. And for 2-Lane case (LANSEL[1:0]=01), the D3P/N and D2P/N are not active.												

4.4 Interface Logic Pins

Signal	I/O	Function															
RSTN	I	This signal will reset the device and must be applied to properly initialize the chip. Signal is active low.															
IM[1:0]	I	Interface type selection. The connections of IM[1:0] which not shown in table are invalid. <table><tr><td>IM[:0]</td><td>Display Data</td><td>Command</td></tr><tr><td>00</td><td>MIPI DSI,</td><td>MIPI DSI or 16-bit SPI</td></tr><tr><td>01</td><td>N/A</td><td>9-bit SPI3 (SCL rising edge trigger), SDI/SDO</td></tr><tr><td>10</td><td>N/A</td><td>8-bit SPI4 (SCL rising edge trigger), SDI/SDO</td></tr><tr><td>11</td><td>N/A</td><td>16-bit SPI</td></tr></table>	IM[:0]	Display Data	Command	00	MIPI DSI,	MIPI DSI or 16-bit SPI	01	N/A	9-bit SPI3 (SCL rising edge trigger), SDI/SDO	10	N/A	8-bit SPI4 (SCL rising edge trigger), SDI/SDO	11	N/A	16-bit SPI
IM[:0]	Display Data	Command															
00	MIPI DSI,	MIPI DSI or 16-bit SPI															
01	N/A	9-bit SPI3 (SCL rising edge trigger), SDI/SDO															
10	N/A	8-bit SPI4 (SCL rising edge trigger), SDI/SDO															
11	N/A	16-bit SPI															
BSTM[2:0]	I	Boost mode selection pin. <table><tr><td colspan="3">BSTM[2:0]</td><td>Mode (Default= 111)</td></tr><tr><td>0</td><td>0</td><td>0</td><td>4PWR (VDDI, VDD, AVDD, AVEE) AVDD: by external power AVEE: by external power</td></tr><tr><td>1</td><td>1</td><td>1</td><td>3PWR (VDDI, VDD, AVDD) AVDD: enabled by OLED_EN AVEE: by internal CP</td></tr></table>	BSTM[2:0]			Mode (Default= 111)	0	0	0	4PWR (VDDI, VDD, AVDD, AVEE) AVDD: by external power AVEE: by external power	1	1	1	3PWR (VDDI, VDD, AVDD) AVDD: enabled by OLED_EN AVEE: by internal CP			
BSTM[2:0]			Mode (Default= 111)														
0	0	0	4PWR (VDDI, VDD, AVDD, AVEE) AVDD: by external power AVEE: by external power														
1	1	1	3PWR (VDDI, VDD, AVDD) AVDD: enabled by OLED_EN AVEE: by internal CP														
BIST_EN	I	Normal/BIST/model selection by BIST_EN: 0: Normal Mode 1: BIST Mode (Please connect to “L” for Normal Operation)															
SWIRE	O	Swire protocol setting pin (Note: “H” = VDDI level, “L” = VSSI level.)															
OLED_EN	O	Power IC enable control pin (Note: “H” = VDDI level, “L” = VSSI level.)															
TE_R TE_L	O	Tearing effect output pin to synchronize MCU to frame writing, activated by S/W command. When this pin is not activated, this pin is output low. If not used, please open this pin.															

NOTE: "1" = VDDI level, "0" = VSSI level.

4.5 Driver Output Pins (Pins for Panel)

Signal	I/O	Function
S[1:2160]	O	Pixel electrode driving output
GOUT[1:12]	O	GOA control signals, Level shift output, (VGHR-VGLR)
GOUT[13:24]	O	GOA control signals, Level shift output, (VGHR-VGLR)

4.6 DC/DC Converter Pins

Signal	I/O	Function
AVEE	O	Output voltage from step-up circuit 2, generated from AVDD. Connect a capacitor for stabilization.
VCL	O	Output voltage from step-up circuit 3, generated from VDDDB. Connect a capacitor for stabilization.
VGH	O	Output voltage from step-up circuit 4. Connect a capacitor for stabilization.
VGL	O	Output voltage from step-up circuit 5. Connect a capacitor for stabilization.
C21P, C21N C22P, C22N	I/O	Capacitor connection pins for the step-up circuit to generate VGH. Connect capacitor as requirement. When not in used, please open these pins.
C23P, C23N C24P, C24N	I/O	Capacitor connection pins for the step-up circuit to generate VGL. Connect capacitor as requirement. When not in used, please open these pins.
C41P, C41N	I/O	Capacitor connection pins for the step-up circuit to generate VCL Connect capacitor as requirement.
C51P, C51N	I/O	Capacitor connection pins for the step-up circuit to generate AVEE Connect capacitor as requirement.
VGHR	O	Output voltage generated from VGH. LDO output used for panel voltage. Connect a capacitor for stabilization. When not in use, please open this pin.
VGLR	O	Output voltage generated from VGL. LDO output used for panel voltage. Connect a capacitor for stabilization. When not in use, please open this pin.
VGMP	O	Output voltage generated from AVDD. LDO output for gamma high voltage generator.
VGSP	O	Output voltage generated from AVDD. LDO output for gamma low voltage generator.
VREF	O	Regulator output for internal reference voltage. Connect capacitor for stabilization.
DVDD	O	Regulator output for logic system power. Connect a capacitor for stabilization.
MVDDA	O	Regulator output for internal MIPI/MDDI analog system (1.2V typical) Connect a capacitor for stabilization. If not use MIPI or MDDI interface, please open this pin.
VREFN5	O	Regulator output for VREFN5 (-0.2~- -6V)

4.7 Pass Pins

Signal	I/O	Function
PATH1	I/O	Pass Pin (The PATH1 of ILB Pin is internally connected to that of OLB)
PATH3	I/O	Pass Pin (The PATH3 of ILB Pin is internally connected to that of OLB)
PADA	I/O	Pass Pin (The PADA of ILB Pin is internally connected to that of OLB)
PADB	I/O	Pass Pin (The PADB of ILB Pin is internally connected to that of OLB)

4.8 Test Pins

Signal	I/O	Function
S[N]_DUMMY (N=0, 2161, 2162)	O	Test pin. Not accessible to user. Must be left open. (Do not connect to any routing line on the panel)
ANA_TEST[1:0]	O	Test pin. Not accessible to user. Must be left open.
TEST[1:14]	I/O	Test pins. Not accessible to user. Must be left open.
DE	I	Test pin. This pin is not used, please connect to VSSI.
VS	I	Test pin. This pin is not used, please connect to VSSI.
HS	I	Test pin. This pin is not used, please connect to VSSI.
PCLK	I	Test pin. This pin is not used, please connect to VSSI.
D[7:0]	I	Test pins. These pins are not used, please connect to VSSI.
DB_MODE[2:0]	I	Test pins. Not accessible to user. Must be left open or connect to VSSI.
DUMMY[1:350]	I	Dummy pins. These pins are not used.

5. Function Description

5.1 Interface Type Selection

Interface type selection. The connections of IM[1:0] which not shown in table are invalid.

IM[1:0]	Display Data	Command
00	MIPI DSI,	MIPI DSI or 16-bit SPI
01	N/A	9-bit SPI3 (SCL rising edge trigger), SDI/SDO
10	N/A	8-bit SPI4 (SCL rising edge trigger), SDI/SDO
11	N/A	16-bit SPI

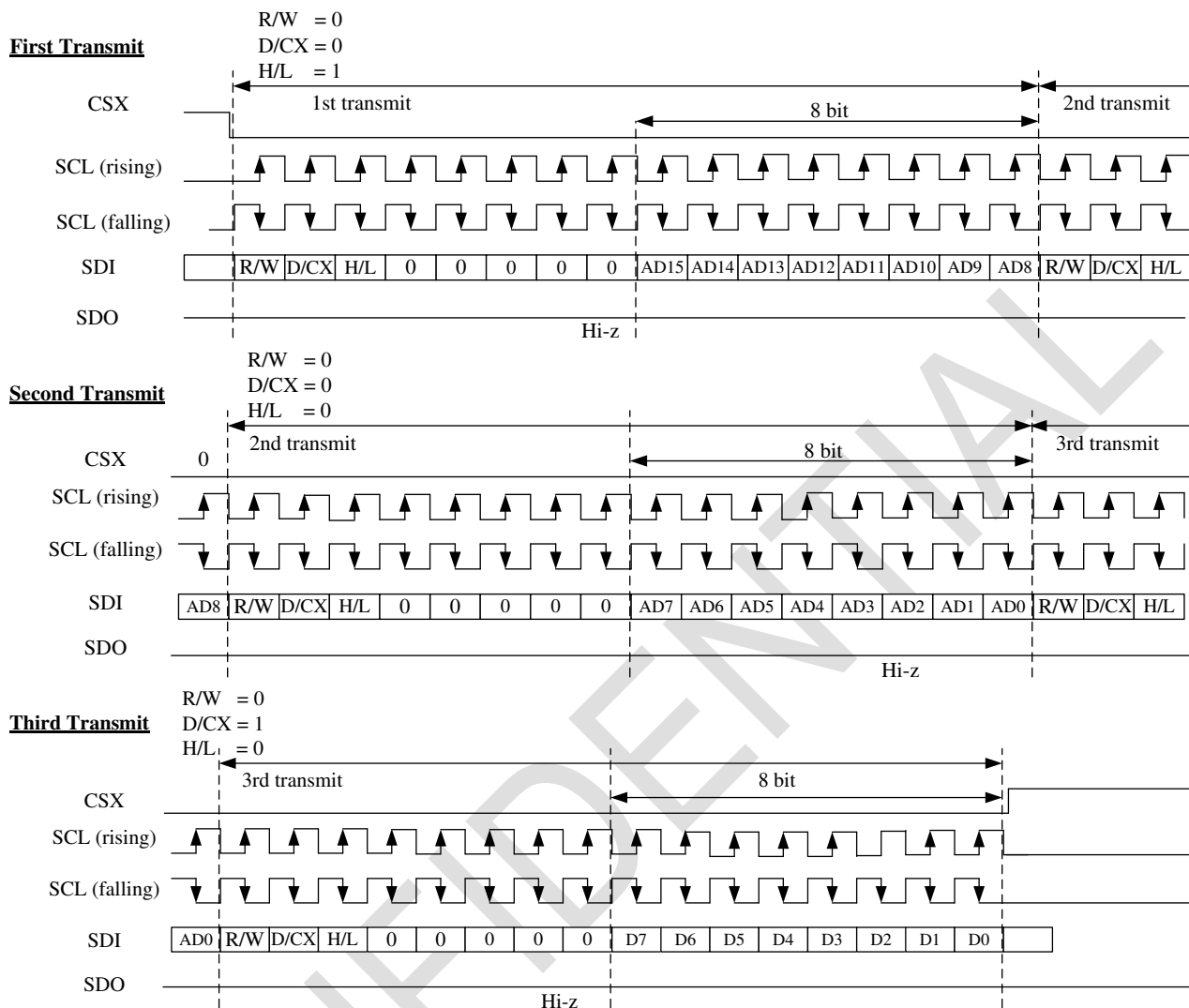
5.2 Serial Interface

5.2.1 Write Cycle and Sequence

During a write cycle the host processor sends a single bit of data to the display module via the interface. The SPI interface utilizes CSX, SCL and SDI and SDO signals. SCL is driven from high to low then pulled back to high during the write cycle. The host processor provides information during the write cycle while the display module reads the host processor information on the rising edge of SCL.

During the write sequence the host processor writes one or more bytes of information to the display module via the interface. The write sequence is initiated when CSX is driven from high to low and ends when CSX is pulled high. Each byte is either nine or sixteen write cycles in length. If the optional DCX signal is used a byte is eight write cycles long. DCX is driven low while command information is on the interface and is pulled high when data is present.

The SPI interface write command sequences are described in the following figure.

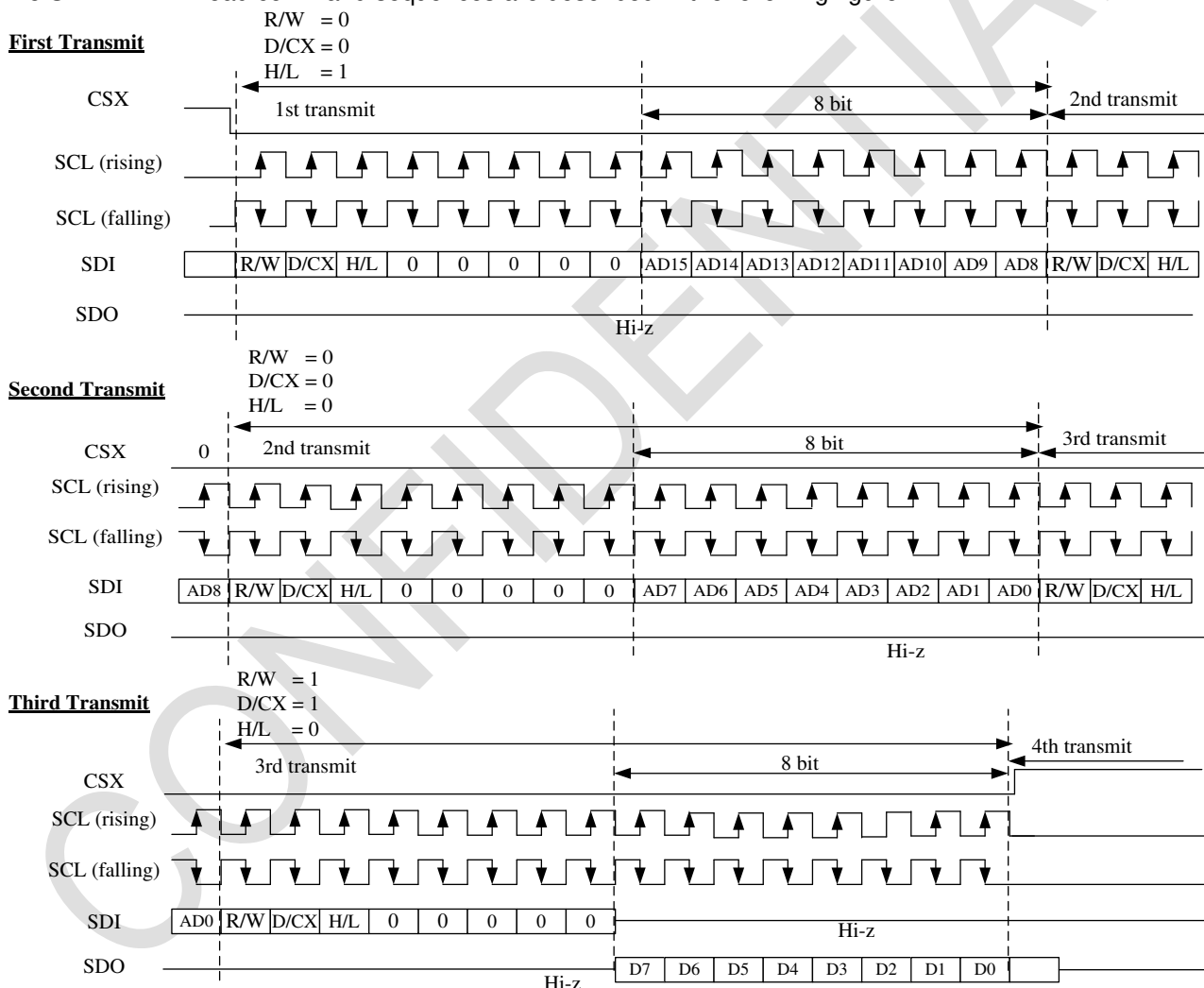


5.2.2 Read Cycle and Sequence

During a read cycle the host processor reads a single bit of data from the display module via the interface. The SPI interface utilizes CSX, SCL and DIN signals. SCL is driven from high to low then pulled back to high during the read cycle. The display module provides information during the read cycle while the host processor reads the display module information on the rising edge of SCL.

During the read sequence the host processor reads one or more bytes of information from the display module via the interface. The read sequence is initiated when CSX is driven from high to low and ends when CSX is pulled high. Each byte is either nine or sixteen write cycles in length. If the optional DCX signal is used a byte is eight read cycles long. DCX is driven low while command information is on the interface and is pulled high when data is present.

The SPI interface read command sequences are described in the following figure.

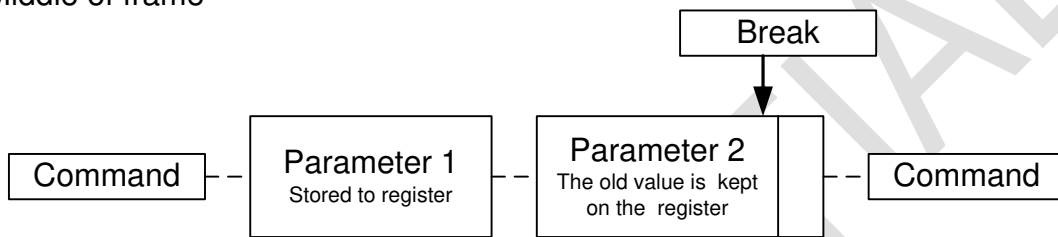


5.2.3 Break and Pause Sequence

The host processor can break a read or write sequence by pulling the CSX signal high during a command or data byte. The display module shall reset its interface so it will be ready to receive the same byte when CSX is again driven low.

The host processor can pause a read or write sequence by pulling the CSX signal high between command and data bytes. The display module shall wait for the host processor to drive CSX low before continuing the read or write sequence at the point where the sequence was paused.

1. Middle of frame

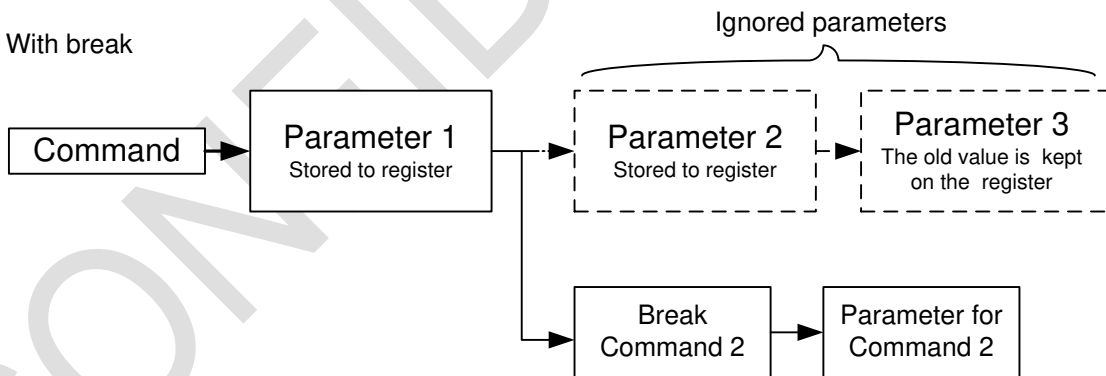


2. Between frames

Without break



With break



Break can be e.g. another command or noise pulse.

5.3 Display Serial Interface (DSI)

DSI-compliant peripherals support either of two basic modes of operation: Command Mode and Video Mode. The mode definitions reflect the primary intended use of DSI for display interconnect, but are not intended to restrict DSI from operating in other applications.

RM67295 is capable of both Command Mode operation and Video Mode operation. Command Mode refers to operation in which transactions primarily take the form of sending commands to a display module that incorporates a display controller. The display controller may include local registers. Systems using Command Mode write to, and read from, the registers. The host processor indirectly controls activity at the peripheral by sending commands and parameters to the display controller.

The host processor can also read display module status information. Command Mode operation requires a bidirectional interface. Video Mode refers to operation in which transfers from the host processor to the peripheral take the form of a real-time pixel stream. In normal operation, the display module relies on the host processor to provide image data at sufficient bandwidth to avoid flicker or other visible artifacts in the displayed image. Video information should only be transmitted using High Speed Mode.

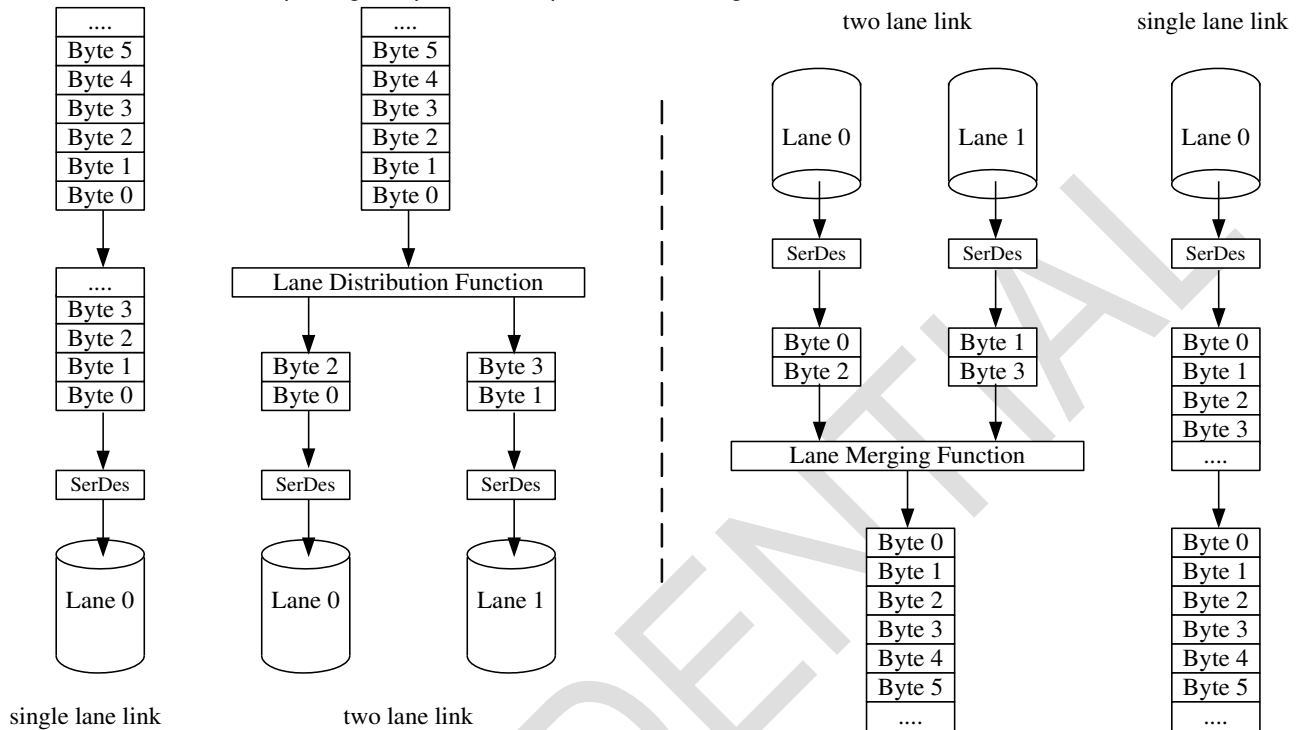
RM67295 Video Mode architectures also include a simple timing controller and partial frame buffer, used to maintain a partial-screen or lower-resolution image in standby or Low Power Mode. This permits the interface to reduce power consumption.

RM67295 Configuration:

Lane Pair	MCU(Master) RM67295(Slave)
Clock Lane	Unidirectional Lane Clock only
Data Lane 0	Bi-directional Lane Forward High-speed Bi-directional Escape Mode Bi-directional LPDT
Data Lane 1	Unidirectional Lane Forward High-Speed Escape Mode No LPDT
Data Lane 2	Unidirectional Lane Forward High-speed Escape Mode No LPDT
Data Lane 3	Unidirectional Lane Forward High-speed Escape Mode No LPDT

5.3.1 DSI Protocol

On the transmitter side of a DSI Link, parallel data, signal events, and commands are converted to packets. These packets are sent across the serial Link. The receiver side of a DSI Link performs the converse of the transmitter side, decomposing the packet into parallel data, signal events and commands.



There are two kinds of packets, **short packet and long packet**.

Short packet structure:

LP-11: low power mode

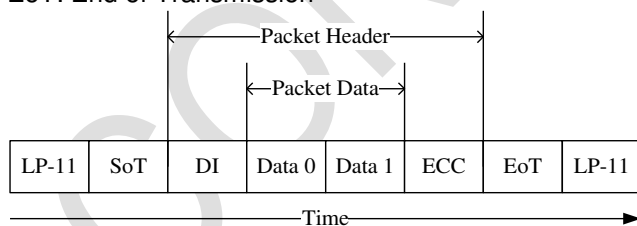
SoT: start of transmission

DI: data identification

Data 0, Data1: packet data

ECC: error correction code

EoT: End of Transmission



DI structure:

Virtual Channel: these two bits identify the data as directed to one of four virtual channels

Data Type: It specifies the packet structure and packet format

Virtual Channel (VC)		Data Type (DT)					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Long packet structure:

LP-11: low power mode

SoT: start of transmission

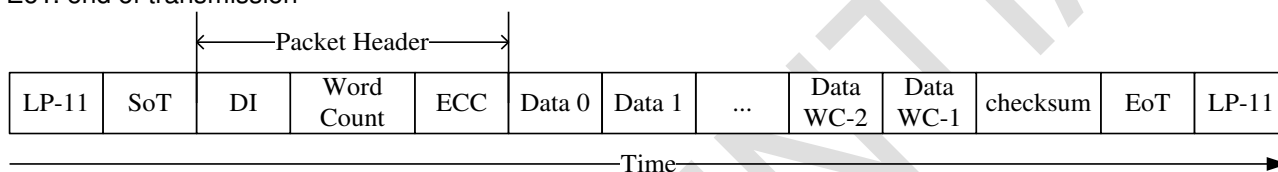
DI: data identification

Word Count: the number of data bytes of packet data

ECC: error correction code

Checksum: The 16-bit CRC generator to check packet data. If the calculated checksum of receiver are equal to the packet data, the packet data is correct. If the calculated checksum of receiver are not equal, the packet data are not correct.

EoT: end of transmission



5.3.2 Processor to Peripheral Transactions

Processor to Peripheral Direction Packet Data Types

Data Type	Data Type binary	Description	Packet Size
01h	00 0001	Sync Event, V Sync Start	Short
11h	01 0001	Sync Event, V Sync End	Short
21h	10 0001	Sync Event, H Sync Start	Short
31h	11 0001	Sync Event, H Sync End	Short
08h	00 1000	End of Transmission packet (EoTp)	Short
02h	00 0010	Color Mode (CM) Off Command	Short
12h	01 0010	Color Mode (CM) On Command	Short
22h	10 0010	reserved	Short
32h	11 0010	reserved	Short
03h	00 0011	reserved	Short
13h	01 0011	Generic Short WRITE, 1 parameter	Short
23h	10 0011	Generic Short WRITE, 2 parameters	Short
04h	00 0100	reserved	Short
14h	01 0100	Generic READ, 1 parameter	Short
24h	10 0100	Generic READ, 2 parameters	Short
05h	00 0101	DCS Short WRITE, no parameters	Short
15h	01 0101	DCS Short WRITE, 1 parameter	Short
06h	00 0110	DCS READ, no parameters	Short
37h	11 0111	Set Maximum Return Packet Size	Short
09h	00 1001	Null Packet, no data	Long
19h	01 1001	Blanking Packet, no data	Long
29h	10 1001	Generic Long Write	Long
39h	11 1001	DCS Long Write/write_LUT Command Packet	Long
0Eh	00 1110	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	Long
1Eh	01 1110	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
2Eh	10 1110	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
3Eh	11 1110	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	Long

Sync Event, Data Type = xx 0001

Sync Events are all short packets and time-accurately. They can perform like the start and end of sync pulses. To represent timing information as accurately as possible, a V Sync Start event represents the start of the VSA and also implies an H Sync Start event for the first line of the VSA. Hence, a V Sync End event implies an H Sync Start event for the last line of the VSA. Sync events may be concatenated with blanking packets to convey inter-line timing accurately and avoid the overhead of switching between LPS and HS for every event. Note there is a power penalty for keeping the data line in HS mode.

EoT packet

This short packet is used to indicate the end of a high speed (HS) transmission. This packet will enhance overall system reliability. Although the main objective of the EoTp is to enhance robustness during HS transmission mode, RM67295 can detect and interpret arriving EoTps regardless of transmission mode (HS or LP modes)

Color Mode Off / On Command

They are short packet commands to switch video display module between normal display mode and low-color mode for power saving.

Generic short write / read packet

Generic Short WRITE command is a Short packet type for sending generic data to the peripheral. Generic READ request is a Short packet requesting data from the peripheral.

DCS commands**DCS short write command**

DCS short write command is used to write a single data byte command to display module. If there is a valid parameter byte, data type bit 4 shall be set to 1. If there is no valid parameter byte, data type bit 4 shall be set to 0 and the parameter byte shall be 00h.

DCS read commands

The commands are used to request data from a display module.

DCS Long Write / write_LUT command

The commands are used to send larger blocks of data to a display module.

Maximum return packet size

This command specifies the maximum size of the payload in a long packet transmission from a display module to host processor.

Null Packet

This is a mechanism for keeping the data lane(s) in high speed mode while sending dummy data.

Blanking Packet

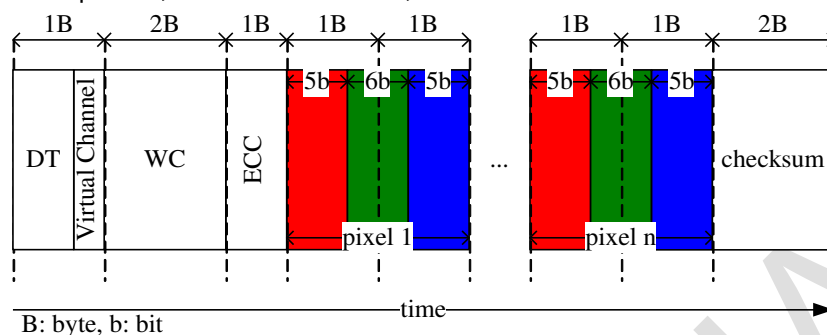
A Blanking packet is used to convey blanking timing information in a Long packet. The packet represents a period between active scan lines of a Video Mode display, where traditional display timing is provided from the host processor to the display module. The blanking period may have Sync Event packets interspersed between blanking segments. Blanking packets may contain arbitrary data as payload.

Generic Long Write

This is used to transmit arbitrary blocks of data from a host processor to a peripheral.

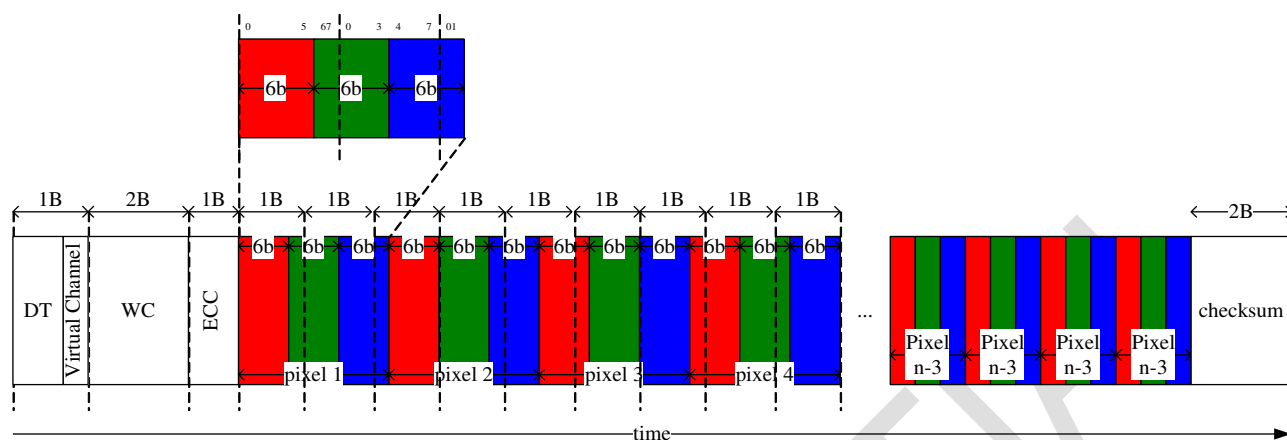
Packed Pixel Stream, 16-bit Format, Data Type: 00 1110

The pixel format is five bits red, six bits green and five bits blue. The green component is split across two bytes. Within a color component, the LSB is sent first, the MSB last.



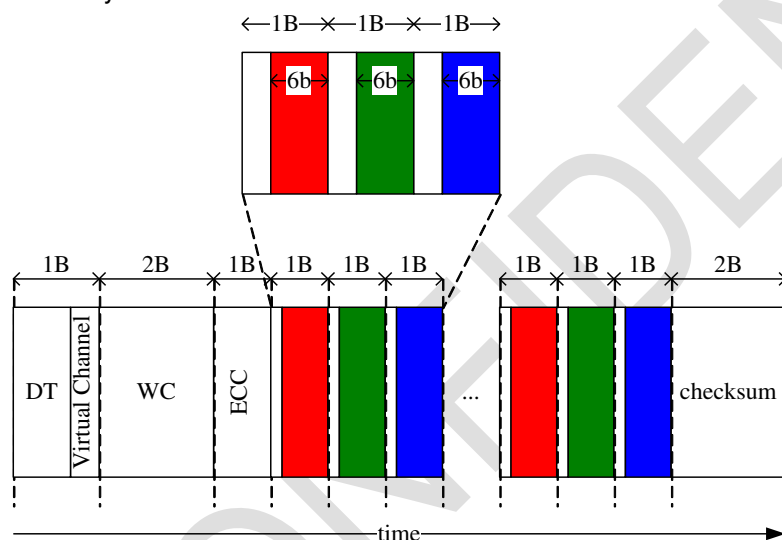
Packet pixel stream, 18-bit format, Data Type: 01 1110

The pixel format is six bits red, six bits green and six bits blue. Within a color component, the LSB is sent first, the MSB last.

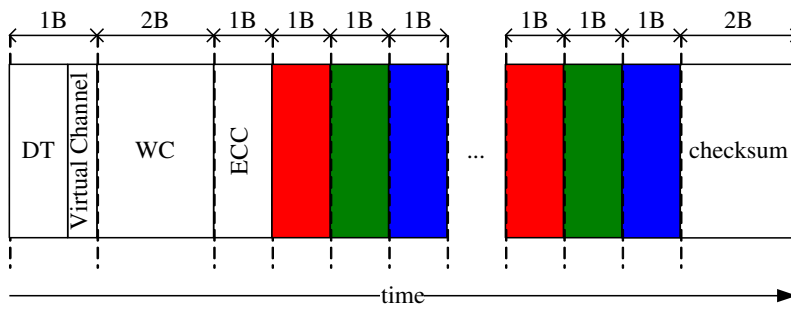


Packet pixel stream, 18-bit format in three bytes, Data Type: 10 1110

This is 18-bit pixel lossely packed format, each R, G or B color component is six bits but shifted to the upper bits of byte.



Packet pixel stream, 24-bit format, Data Type: 11 1110
The pixel format is eight bits red, eight bits green and eight bits blue.



5.3.3 Peripheral-to-Processor LP Transmission

All Command Mode systems require bidirectional capability for returning READ data, acknowledge, or error information to the host processor. Multi-Lane systems shall use Lane 0 for all peripheral-to-processor transmissions. Reverse-direction signaling shall only use low power mode transmission.

Packet structure for peripheral-to-processor transaction is the same as for the processor-to-peripheral direction. For the processor-to-peripheral direction, two basic packet formats are the same as the peripheral-to-processor direction: Short and Long packet structure. BTA shall take place after every peripheral-to-processor transaction. This returns bus control to the host processor following the completion of the LP transmission from the peripheral.

There are four basic types of peripheral-to-processor transactions.

Tearing Effect: It is a Trigger message sent to convey display timing information to the host processor.

Acknowledge: It is a Trigger Message sent when the current transmission, as well as all preceding transmissions since the last peripheral to host communication.

Acknowledge and Error Report: It is a Short packet sent if any errors were detected in preceding transmissions from the host processor.

Response to Read Request: It may be a Short or Long packet that returns data requested by the preceding READ command from the processor.

Interpretation of processor-to-peripheral transactions with BTA asserted, and the expected responses, are as follows:

Following a non-Read command: If no errors were detected, the peripheral shall respond with Acknowledge.

Following a Read request: The peripheral shall send the requested READ data if no errors were detected and stored since the last peripheral to host communication.

Following a Read request: If only a single-bit ECC error was detected and corrected, the peripheral shall send the requested READ data in a Long or Short packet and a 4-byte Acknowledge and Error Report packet in the same LP transmission.

Following a non-Read command: If only a single-bit ECC error was detected and corrected, the peripheral shall respond to BTA by sending a 4-byte Acknowledge and Error Report packet.

Following a Read request: If multi-bit ECC errors were detected and not corrected, the peripheral shall send a 4-byte Acknowledge and Error Report packet without sending Read data.

Following a non-Read command: If multi-bit ECC errors were detected and not corrected, the peripheral shall not execute the command, and shall send a 4-byte Acknowledge and Error Report packet.

Following any command: If SoT Error, SoT Sync Error, the VC of DSI or the ID of DSI Invalid or DSI protocol violation was detected, or the DSI command was not recognized, the peripheral shall send a 4-byte Acknowledge and Error Report response.

Following any command: If EoT Sync Error or LP Transmit Sync Error is detected, or a checksum error is detected in the payload, the peripheral shall send a 4-byte Acknowledge and Error Report packet.

Error Report Format

The following table shows the bit assignment for all error report.

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	HS Receive Timeout Error
6	False Control Error
7	Reserved
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error (Long packet only)
11	DSI Data Type Not Recognized
12	DSI VC ID Invalid
13	reserved
14	reserved
15	reserved

Peripheral-to-Processor Transaction – Detail Format Description

The following list is the complete set of peripheral-to-processor data types.

Data type, hex	Data type binary	Description	Packet size
02h	00 0010	Acknowledge and error report	short
08h	00 1000	reserved	short
11h	01 0001	GEN short read response, 1byte returned	short
12h	01 0010	GEN short read response, 2bytes returned	short
1Ah	01 1010	Generic long read response	long
1Ch	01 1100	DCS long read response	long
21h	10 0001	DCS short read response, 1byte returned	short
22h	10 0010	DCS short read response, 2bytes returned	short

Acknowledge and error report: It is sent with BTA asserted when a reportable error is detected in the preceding, or earlier, transmission from the host processor.

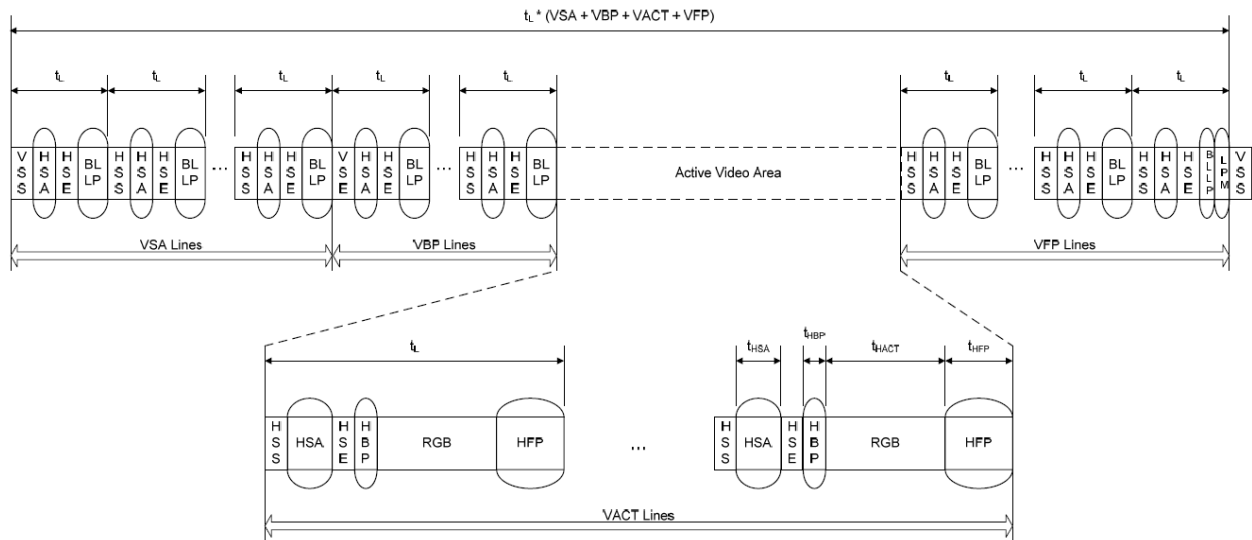
Generic Short Read response: This is the short-packet response to Generic READ Request. Packet composition is the Data Identifier (DI) byte, two bytes of payload data and an ECC byte. If the command itself is possibly corrupt, due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent and only the Acknowledge and Error Report packet shall be sent.

Generic long read response: This is the long-packet response to Generic READ Request. Packet composition is DI followed by a two-byte Word Count, an ECC byte, N bytes of payload, and a two-byte Checksum. If the command itself is possibly corrupt, due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent and only the Acknowledge and Error Report packet shall be sent.

DCS long read response: This is a Long packet response to DCS Read Request. Packet composition is DI followed by a two-byte Word Count, an ECC byte, N bytes of payload, and a two-byte Checksum. If the DCS command itself is possibly corrupt, due to uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent and only the Acknowledge and Error Report packet shall be sent.

DCS short read response: This is the short-packet response to DCS Read Request. Packet composition is DI, two bytes of payload data and an ECC byte. If the command itself is possibly corrupt, due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent and only the Acknowledge and Error Report packet shall be sent.

5.3.4 DSI Video Mode Interface Timing



5.3.5 Error Correction Code (ECC)

ECC shall always be generated and appended in the Packet Header from the host processor. Peripherals with Bidirectional Links shall also generate and send ECC.

The number of parity or error check bits required is given by the Hamming rule, which uses parity to correct a single-bit error or detect a two-bit error, but are not capable of doing both simultaneously. DSI uses Hamming-modified codes where an extra parity bit is used to support both single error correction as well as two-bit error detection.

Since Packet Headers are fixed at four bytes (twenty-four data bits and eight ECC bits), P6 and P7 of the ECC byte are unused and shall be set to zero by the transmitter. The receiver shall ignore P6 and P7 and set both bits to zero before processing ECC.

The parity bits of ECC are defined as below:

$$P7 = 0$$

$$P6 = 0$$

$$P5 = D10 \oplus D11 \oplus D12 \oplus D13 \oplus D14 \oplus D15 \oplus D16 \oplus D17 \oplus D18 \oplus D19 \oplus D21 \oplus D22 \oplus D23$$

$$P4 = D4 \oplus D5 \oplus D6 \oplus D7 \oplus D8 \oplus D9 \oplus D16 \oplus D17 \oplus D18 \oplus D19 \oplus D20 \oplus D22 \oplus D23$$

$$P3 = D1 \oplus D2 \oplus D3 \oplus D7 \oplus D8 \oplus D9 \oplus D13 \oplus D14 \oplus D15 \oplus D19 \oplus D20 \oplus D21 \oplus D23$$

$$P2 = D0 \oplus D2 \oplus D3 \oplus D5 \oplus D6 \oplus D9 \oplus D11 \oplus D12 \oplus D15 \oplus D18 \oplus D20 \oplus D21 \oplus D22$$

$$P1 = D0 \oplus D1 \oplus D3 \oplus D4 \oplus D6 \oplus D8 \oplus D10 \oplus D12 \oplus D14 \oplus D17 \oplus D20 \oplus D21 \oplus D22 \oplus D23$$

$$P0 = D0 \oplus D1 \oplus D2 \oplus D4 \oplus D5 \oplus D7 \oplus D10 \oplus D11 \oplus D13 \oplus D16 \oplus D20 \oplus D21 \oplus D22 \oplus D23$$

The table below shows a compact way to specify the encoding of parity and decoding of syndromes.

ECC Parity Generation Rules:

Data Bit	P7	P6	P5	P4	P3	P2	P1	P0	Hex
0	0	0	0	0	0	1	1	1	0x07
1	0	0	0	0	1	0	1	1	0x0B
2	0	0	0	0	1	1	0	1	0x0D
3	0	0	0	0	1	1	1	0	0x0E
4	0	0	0	1	0	0	1	1	0x13
5	0	0	0	1	0	1	0	1	0x15
6	0	0	0	1	0	1	1	0	0x16
7	0	0	0	1	1	0	0	1	0x19
8	0	0	0	1	1	0	1	0	0x1A
9	0	0	0	1	1	1	0	0	0x1C
10	0	0	1	0	0	0	1	1	0x23
11	0	0	1	0	0	1	0	1	0x25
12	0	0	1	0	0	1	1	0	0x26
13	0	0	1	0	1	0	0	1	0x29
14	0	0	1	0	1	0	1	0	0x2A
15	0	0	1	0	1	1	0	0	0x2C
16	0	0	1	1	0	0	0	1	0x31
17	0	0	1	1	0	0	1	0	0x32
18	0	0	1	1	0	1	0	0	0x34
19	0	0	1	1	1	0	0	0	0x38
20	0	0	0	1	1	1	1	1	0x1F
21	0	0	1	0	1	1	1	1	0x2F
22	0	0	1	1	0	1	1	1	0x37
23	0	0	1	1	1	0	1	1	0x3B

5.3.6 Notice

1. We recommend users to stay in STOP state for 500ns when switching from LPDT to HSDT.
2. We recommend users to adopt EoT to enhance overall robustness of the system during HSDT.

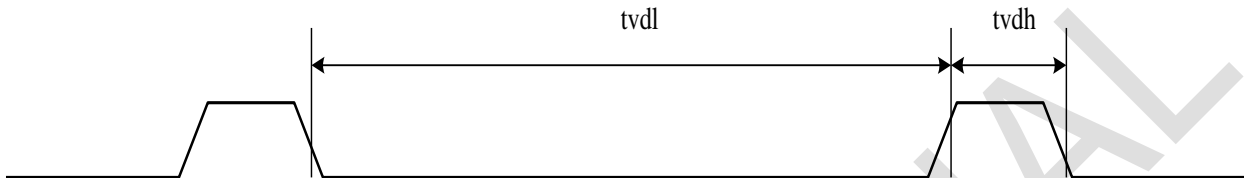
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5.4 Tearing Effect Output

The tearing effect output line supplies to the HOST a panel synchronization signal. This signal can be enabled or disabled by the set_tear_off (34h) and set_tear_on (35h) commands. The mode of the tearing effect signal is defined by the parameter of the set_tear_on (35h) and set_tear_scanline(44h) commands. The signal can be used by the HOST to synchronize internal VSYNC when displaying video images.

5.4.1 Tearing Effect Line Mode

Mode 1, the tearing effect output signal consist of V-sync information only:



tvdh = The LCD display is not updated from the frame memory.

tvdl = The LCD display is updated from the frame memory.

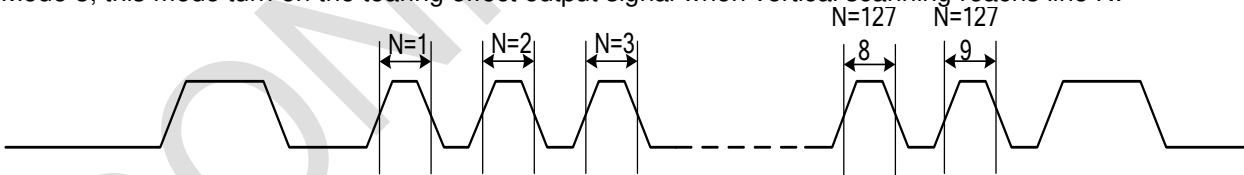
Mode 2, the tearing effect output signal consist of V-sync and H-sync information:



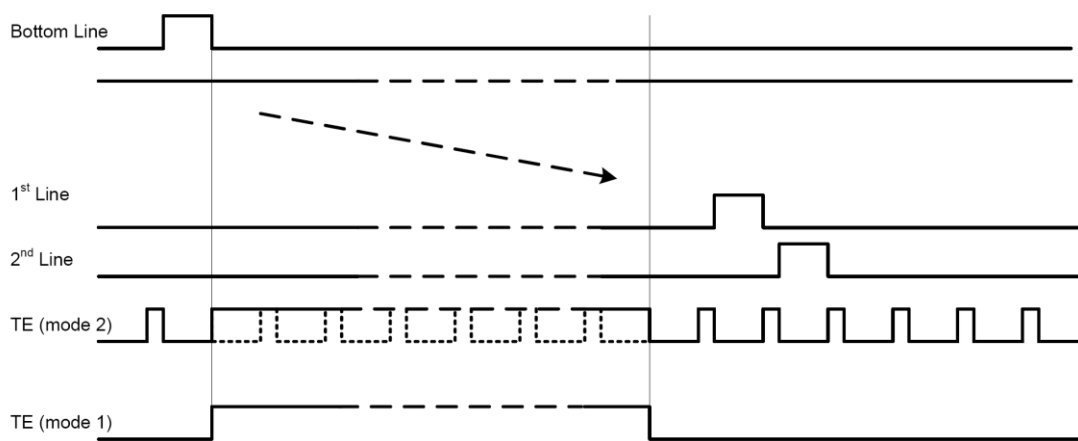
thdh = The LCD display is not updated from the frame memory.

thdl = The LCD display is updated from the frame memory.

Mode 3, this mode turn on the tearing effect output signal when vertical scanning reaches line N.



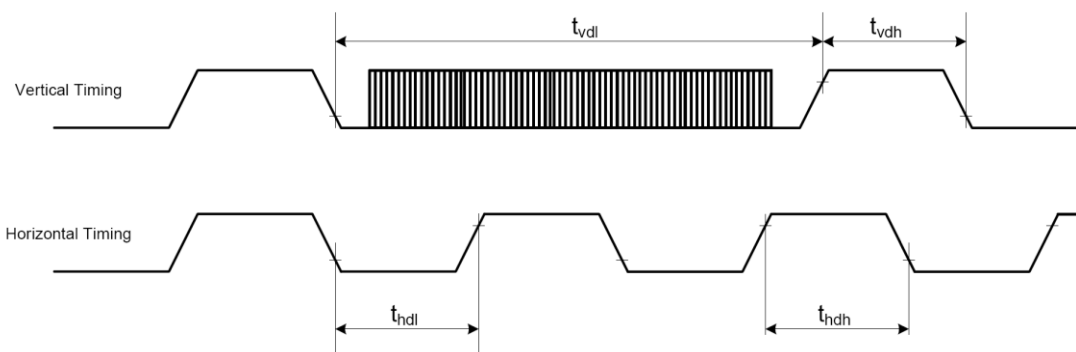
N = The N-th scanning line which set by register N[15:0] of command STESL(44h).



Note. During Sleep In mode, the tearing effect output signal is active low.

5.4.2 Tearing Effect Line Timing

The tearing effect signal is described as below:

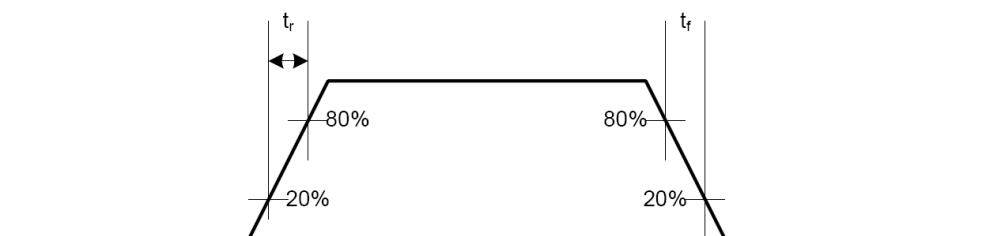


AC characteristics of Tearing Effect Signal (Frame Rate = 60.5Hz)

Symbol	Parameter	Min.	Max.	Unit	Description
t_{vdl}	Vertical timing low duration	TBD		ms	
t_{vdh}	Vertical timing high duration	TBD		us	
t_{hdl}	Horizontal timing low duration	TBD		us	
t_{hdh}	Horizontal timing high duration	TBD		us	

Notes:

1. The timings apply when MADCTL B4=0 and B4=1
2. The signal's rise and fall times (t_f , t_r) are stipulated to be equal to or less than 15ns.



The Tearing Effect Output Line is fed back to the HOST and should be used as shown below to avoid tearing effect:

The Tearing Effect output line supplies to the HOST a panel synchronization signal. This signal can be enabled or disabled by the `set_tear_off(34h)`, `set_tear_on(35h)` commands. The mode of the Tearing Effect Signal is defined by the Parameter of the Tearing Effect Line On command. The signal can be used by the HOST to synchronize internal VSYNC when displaying video images.

TEON (35h)	TELOM (35h, 1 st bit)	TE signal Output
0	*	GND
1	0	TE (Mode 1)
1	1	TE (Mode 2)

6. Command

6.1. Command List

Table of User Command Set (Command 1)

CMD1	Para	Instruction	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	-	Nop	No argument								-
01h	-	Soft reset	No argument								-
04h	00h	Get display ID	ID1[7:0]								00h
	01h		ID2[7:0]								00h
	02h		ID3[7:0]								00h
05h	-	Get number of errors on DSI	D[7:0]								00h
0Ah	00h	Get power mode	BSTON	IDMON	-	SLPOUT	-	DISPON	-	-	-
0Bh	00h	Get address mode	-	-	-	-	RGB	-	RSMX	RSMY	00h
0Ch	00h	Get pixel format	-	VIPF2	VIPF1	VIPF0	-	IFPF2	IFPF1	IFPF0	77h
0Dh	00h	Get display mode	-	-	INVON	ALLPON	ALLPOFF	-	-	-	00h
0Eh	00h	Get signal mode	TEON	M	-	-	-	-	-	ERR	00h
0Fh	00h	Get diagnostic result	D7	D6	D5	D4	-	-	-	-	00h
10h	-	Enter sleep mode	No argument								-
11h	-	Exit sleep mode	No argument								-
20h	-	Exit invert mode	No argument								-
21h	-	Enter invert mode	No argument								-
22h	-	Set all pixels off	No argument								-
23h	-	Set all pixels on	No argument								-
28h	-	Set display off	No argument								-
29h	-	Set display on	No argument								-
34h	-	Set tear off	No argument								-
35h	00h	Set tear on	-	-	-	-	-	-	-	TELOM	00h
36h	00h	Set address mode	-	-	-	-	RGB	-	RSMX	RSMY	00h
38h	-	Exit idle mode	No argument								-
39h	-	Enter idle mode	No argument								-
3Ah	00h	Set pixel format	-	VIPF2	VIPF1	VIPF0	-	IFPF2	IFPF1	IFPF0	77h
44h	00h	Set tear scan line	N[15:8]								00h
	01h		N[7:0]								00h
45h	00h	Get scan line	N[15:8]								00h
	01h		N[7:0]								00h
4Fh	00h	Set deep standby mode	-	-	-	-	-	-	-	DSTB	00h
51h	00h	Write display brightness	DBV[7:0] (input)								FFh
52h	00h	Read display brightness	DBV[7:0] (output)								FFh

53h	00h	Write control display	HBM[1:0]		BCTRL	-	DD	-	-		20h
54h	00h	Read control display	-	-	BCTRL	-	DD	-	-		20h
55h	00h	Write RAD-ACL control	-	-	-	-	-	-	RAD_ACL[1:0]		00h
56h	00h	Read RAD-ACL control	-	-	-	-	-	-	RAD_ACL[1:0]		00h
58h	00h	Write CE	CTE_EN	CTE_LEVEL[3:0]				CTE_SLR_EN	-		48h
59h	00h	Read CE	CTE_EN	CTE_LEVEL[3:0]				CTE_SLR_EN	-		48h
5Ah	00h	Write CE1	SKIN_EN	-	SKIN_LEVEL[1:0]	EN_VIVID_ENH	-	CE_LEVEL[1:0]		11h	
5Bh	00h	Read CE1	SKIN_EN	-	SKIN_LEVEL[1:0]	EN_VIVID_ENH	-	CE_LEVEL[1:0]		11h	
5Ch	00h	Write CE2	SLR_EN	-	SLR_LEVEL[1:0]	EN_EDGE	EDGE_LEVEL[2:0]				14h
5Dh	00h	Read CE2	SLR_EN	-	SLR_LEVEL[1:0]	EN_EDGE	EDGE_LEVEL[2:0]				14h
62h	00h	Write CE3 (temper)	TEMPER_EN	TEMPER_LEVEL[6:0]							00h
63h	00h	Read CE3 (temper)	TEMPER_EN	TEMPER_LEVEL[6:0]							00h
64h	00h	Write CE4 (paper)	PAPER_EN	PAPER_LEVEL[6:0]							00h
65h	00h	Read CE4 (paper)	PAPER_EN	PAPER_LEVEL[6:0]							00h
66h	00h	Write CE5 (WB)	WB_EN	-							00h
67h	00h	Read CE5 (WB)	WB_EN	-							00h
68h	00h	Write CE6 (CE mode)	-	-	-	-	-	CE_MODE[2:0]		00h	
69h	00h	Read CE6 (CE mode)	-	-	-	-	-	CE_MODE[2:0]		00h	
6Ah	00h	Write HDR	HDR_EN	HDR_LEVEL[6:0]							50h
6Bh	00h	Read HDR	HDR_EN	HDR_LEVEL[6:0]							50h
A1h	00h	Read DDB start	SID[15:8]								00h
	01h		SID[7:0]								00h
	02h		MID[15:8]								00h
	03h		MID[7:0]								00h
	04h		1	1	1	1	1	1	1	1	FFh
A8h	00h	Read DDB continue	SID[15:8]								00h
	01h		SID[7:0]								00h
	02h		MID[15:8]								00h
	03h		MID[7:0]								00h
	04h		1	1	1	1	1	1	1	1	FFh
AAh	00h	Read first checksum	FCS[7:0]								00h
AFh	00h	Read continue checksum	CCS[7:0]								00h
DAh	00h	Read ID1	ID1[7:0]								00h
DBh	00h	Read ID2	ID2[7:0]								00h
DCh	00h	Read ID3	ID3[7:0]								00h
FEh	00h	Write CMD page switch					CMD_PG_SEL[3:0]			00h	

FFh	00h	Read CMD page					CMD_PG_SEL[3:0]	00h
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Table of User Command Set (Command 1) (continued)

CMD1	Para.	Instruction	Status Availability			
			command(C) / read (R) / write (W)	Normal mode on, idle mode off, sleep out	Normal mode on, idle mode on, sleep out	sleep in
00h	-	Nop	C	Yes	Yes	Yes
01h	-	Soft reset	C	Yes	Yes	Yes
04h	00h	Get display ID	R	Yes	Yes	Yes
	01h		R	Yes	Yes	Yes
	02h		R	Yes	Yes	Yes
05h	-	Get number of errors on DSI	R	Yes	Yes	Yes
0Ah	00h	Get power mode	R	Yes	Yes	Yes
0Bh	00h	Get address mode	R	Yes	Yes	Yes
0Ch	00h	Get pixel format	R	Yes	Yes	Yes
0Dh	00h	Get display mode	R	Yes	Yes	Yes
0Eh	00h	Get signal mode	R	Yes	Yes	Yes
0Fh	00h	Get diagnostic result	R	Yes	Yes	Yes
10h	-	Enter sleep mode	C	Yes	Yes	Yes
11h	-	Exit sleep mode	C	Yes	Yes	Yes
20h	-	Exit invert mode	C	Yes	Yes	Yes
21h	-	Enter invert mode	C	Yes	Yes	Yes
22h	-	Set all pixels off	C	Yes	Yes	Yes
23h	-	Set all pixels on	C	Yes	Yes	Yes
28h	-	Set display off	C	Yes	Yes	Yes
29h	-	Set display on	C	Yes	Yes	Yes
34h	-	Set tear off	C	Yes	Yes	Yes
35h	00h	Set tear on	W	Yes	Yes	Yes
36h	00h	Set address mode	W	Yes	Yes	Yes
38h	-	Exit idle mode	C	Yes	Yes	Yes
39h	-	Enter idle mode	C	Yes	Yes	Yes
3Ah	00h	Set pixel format	W	Yes	Yes	Yes
44h	00h	Set tear scan line	W	Yes	Yes	Yes
	01h		W	Yes	Yes	Yes
45h	00h	Get scan line	R	Yes	Yes	Yes
	01h		R	Yes	Yes	Yes
4Fh	00h	Set deep standby mode	W	Yes	Yes	Yes
51h	00h	Write display brightness	W	Yes	Yes	Yes
52h	00h	Read display brightness	R	Yes	Yes	Yes

53h	00h	Write control display	W	Yes	Yes	Yes
54h	00h	Read control display	R	Yes	Yes	Yes
55h	00h	Write RAD-ACL control	W	Yes	Yes	Yes
56h	00h	Read RAD-ACL control	R	Yes	Yes	Yes
58h	00h	Write CE	W	Yes	Yes	Yes
59h	00h	Read CE	R	Yes	Yes	Yes
5Ah	00h	Write CE1	W	Yes	Yes	Yes
5Bh	00h	Read CE1	R	Yes	Yes	Yes
5Ch	00h	Write CE2	W	Yes	Yes	Yes
5Dh	00h	Read CE2	R	Yes	Yes	Yes
62h	00h	Write CE3 (temper)	W	Yes	Yes	Yes
63h	00h	Read CE3 (temper)	R	Yes	Yes	Yes
64h	00h	Write CE4 (paper)	W	Yes	Yes	Yes
65h	00h	Read CE4 (paper)	R	Yes	Yes	Yes
66h	00h	Write CE5 (WB)	W	Yes	Yes	Yes
67h	00h	Read CE5 (WB)	R	Yes	Yes	Yes
68h	00h	Write CE6 (CE mode)	W	Yes	Yes	Yes
69h	00h	Read CE6 (CE mode)	R	Yes	Yes	Yes
6Ah	00h	Write HDR	W	Yes	Yes	Yes
6Bh	00h	Read HDR	R	Yes	Yes	Yes
A1h	00h	Read DDB start	R	Yes	Yes	Yes
	01h		R	Yes	Yes	Yes
	02h		R	Yes	Yes	Yes
	03h		R	Yes	Yes	Yes
	04h		R	Yes	Yes	Yes
A8h	00h	Read DDB continue	R	Yes	Yes	Yes
	01h		R	Yes	Yes	Yes
	02h		R	Yes	Yes	Yes
	03h		R	Yes	Yes	Yes
	04h		R	Yes	Yes	Yes
AAh	00h	Read first checksum	R	Yes	Yes	Yes
AFh	00h	Read continue checksum	R	Yes	Yes	Yes
DAh	00h	Read ID1	R	Yes	Yes	Yes
DBh	00h	Read ID2	R	Yes	Yes	Yes
DCh	00h	Read ID3	R	Yes	Yes	Yes
FEh	00h	Write CMD page switch	W	Yes	Yes	Yes
FFh	00h	Read CMD page	R	Yes	Yes	Yes

6.2. Command Description

NOP (0000h)

0000h	NOP (No Operation)																				
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
		MIPI	Other																		
NOP	W	00h	0000h	No Argument																	
Description	This command is an empty command; it does not have any effect on the display module. X = Don't care.																				
Restriction	None																				
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>SW Reset</td><td>N/A</td></tr><tr><td>HW Reset</td><td>N/A</td></tr></table>													Status	Default Value	Power On Sequence	N/A	SW Reset	N/A	HW Reset	N/A
														Status	Default Value						
														Power On Sequence	N/A						
														SW Reset	N/A						
														HW Reset	N/A						
Flow Chart	None																				

SWRESET(0100h) : Software Reset

0100h	SWRESET(Software Reset)																				
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
		MIPI	Other																		
SWRESET	W	01h	0100h	No Argument																	
Description	When the Software Reset command is written, it causes software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.)																				
Restriction	Software Reset Command cannot be sent during Sleep Out sequence. Any new command is cannot be sent for 10-frame period until the RM67190 enters Sleep-In mode. Do not send any command.																				
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>SW Reset</td><td>N/A</td></tr><tr><td>HW Reset</td><td>N/A</td></tr></table>													Status	Default Value	Power On Sequence	N/A	SW Reset	N/A	HW Reset	N/A
Status	Default Value																				
Power On Sequence	N/A																				
SW Reset	N/A																				
HW Reset	N/A																				
Flow Chart	<div><div><div>SWRESET (01h)</div><div>↓</div><div>Display whole blank screen</div><div>↓</div><div>Set Commands to S/W Default Value</div><div>↓</div><div>Sleep In Mode</div></div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																				

RDDID(0400h~0402h) : Get Display ID

0400~0402h		RDDID																									
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX														
		MIPI	Other																								
RDDID	R	04h	0400h	x	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	00														
			0401h	x	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	00														
			0402h	x	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	00														
Description	The 1 st parameter (ID1): the Module's manufacture ID The 2 nd parameter (ID2): the Module/driver version ID The 3 rd parameter (ID3): the Module/driver ID Note: Commands RDID1/2/3 (DAh/DBh/DCh) read data correspond to the parameter 1, 2, 3 of command 04h, respectively.																										
Restriction	-																										
Default	<table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>After MTP</th><th>Before MTP</th></tr><tr><td>Power On Sequence</td><td>MTP value</td><td>ID1=00h / ID2=00h / ID3=00h</td></tr><tr><td>SW Reset</td><td>MTP value</td><td>ID1=00h / ID2=00h / ID3=00h</td></tr><tr><td>HW Reset</td><td>MTP value</td><td>ID1=00h / ID2=00h / ID3=00h</td></tr></table>													Status	Default Value		After MTP	Before MTP	Power On Sequence	MTP value	ID1=00h / ID2=00h / ID3=00h	SW Reset	MTP value	ID1=00h / ID2=00h / ID3=00h	HW Reset	MTP value	ID1=00h / ID2=00h / ID3=00h
Status	Default Value																										
	After MTP	Before MTP																									
Power On Sequence	MTP value	ID1=00h / ID2=00h / ID3=00h																									
SW Reset	MTP value	ID1=00h / ID2=00h / ID3=00h																									
HW Reset	MTP value	ID1=00h / ID2=00h / ID3=00h																									
Flow Chart	<div><div><div>RDDID (04h)</div><div>Send 1st parameter ID1[7:0]</div><div>Send 2nd parameter ID2[7:0]</div><div>Send 3rd parameter ID3[7:0]</div></div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																										

RDNUMED(0500h) : Get Number of Errors on DSI

0500h				RDNUMED																	
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
		MIPI	Other																		
RDNUMED	R	05h	0500h	x	D7	D6	D5	D4	D3	D2	D1	D0	00								
Description	<p>The first parameter is telling a number of the parity errors on DSI. The more detailed description of the bits is below.</p> <p>D[6:0] bits are telling a number of the parity errors.</p> <p>D[7] is set to “1” if there is overflow with D[6..0] bits.</p> <p>D[7:0] bits are set to “0”s (as well as RDDSM(0Eh)’s D0 are set “0” at the same time) after there is sent the first parameter information (= The read function is completed).</p> <p>This command is used for MIPI DSI only. It is no function for others interface operation.</p>																				
Restriction	-																				
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>SW Reset</td><td>00h</td></tr><tr><td>HW Reset</td><td>00h</td></tr></table>													Status	Default Value	Power On Sequence	00h	SW Reset	00h	HW Reset	00h
Status	Default Value																				
Power On Sequence	00h																				
SW Reset	00h																				
HW Reset	00h																				
Flow Chart	<div><div><div>RDNUMED (05h)</div><div>Send 1st parameter</div><div>P[7:0]=00h RDDSM(0Eh)’s D0 = ‘0’</div></div><div><div>Legend</div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																				

RDDPM (0A00h) : Get Power Mode

0A00h				RDDPM (Read Display Power Mode)																	
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
		MIPI	Other																		
RDDPM	R	0Ah	0A00h	x	D7	D6	D5	D4	D3	D2	D1	D0	08								
Description	This command indicates the current status of the display as described in the table below:																				
	Bit	Symbol	Description		Comment																
	D7	BSTON	Booster Voltage Status		'1'=Booster on, '0'=Booster off																
	D6	IDMON	Idle Mode On/Off		'1' = Idle Mode On, '0' = Idle Mode Off																
	D5	Reserved																			
	D4	SLPON	Sleep In/Out		'1' = Sleep Out, '0' = Sleep In																
	D3	Reserved																			
	D2	DISPON	Display On/Off		'1' = Display On, '0' = Display Off																
	D1	Reserved			0																
	D0	Reserved			0																
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>08h</td></tr><tr><td>SW Reset</td><td>08h</td></tr><tr><td>HW Reset</td><td>08h</td></tr></table>													Status	Default Value	Power On Sequence	08h	SW Reset	08h	HW Reset	08h
	Status	Default Value																			
	Power On Sequence	08h																			
	SW Reset	08h																			
	HW Reset	08h																			
Flow Chart	<div><div><div>Serial I/F Mode</div><div><div>RDDPM (0Ah)</div><div>↓</div><div>Send D[7:0]</div></div></div><div><div>Parallel I/F Mode</div><div><div>RDDPM (0Ah)</div><div>↓</div><div>Dummy Read</div><div>↓</div><div>Send D[7:0]</div></div></div><div>Host Driver</div></div>																				
	<div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																				

RDDMADCTR (0B00h): Get Address Mode

0B00h	RDDMADCTR (Read Display MADCTR)																				
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
		MIPI	Other																		
RDDMADCTR	R	0Bh	0B00h	x	D7	D6	D5	D4	D3	D2	D1	D0	00								
Description	This command indicates the current status of the display as described in the table below:																				
	Bit	Symbol	Description		Comment																
	D7	Reserved			0																
	D6	Reserved			0																
	D5	Reserved			0																
	D4	Reserved			0																
	D3	RGB	RGB/BGR Order		'1' =BGR, (36H-D3 = "1") "0"=RGB, (36H-D3 = "0")																
	D2	Reserved			0																
	D1	RSMX	Horizontal Flip		'0' = Normal display(36H-D1='0') '1' = Flipped display(36H-D1='1')																
	D0	RSMY	Vertical Flip		'0' = Normal display '1' = Reverse display																
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>SW Reset</td><td>No Change</td></tr><tr><td>HW Reset</td><td>00h</td></tr></table>													Status	Default Value	Power On Sequence	00h	SW Reset	No Change	HW Reset	00h
	Status	Default Value																			
	Power On Sequence	00h																			
	SW Reset	No Change																			
	HW Reset	00h																			
Flow Chart	<div><div><div>Serial I/F Mode</div><div>RDDMADCTR (0Bh)</div><div>Send D[7:0]</div></div><div><div>Parallel I/F Mode</div><div>RDDMADCTR (0Bh)</div><div>Dummy Read</div><div>Send D[7:0]</div></div></div> <div>Host Driver</div>																				
	<div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																				

RDDCOLMOD (0C00h): Get Pixel Format

0C00h	RDDCOLMOD (Read Display Pixel Format)																				
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
		MIPI	Other																		
RDDCOLMOD	R	0Ch	0C00h	x	D7	D6	D5	D4	D3	D2	D1	D0	77								
Description	This command indicates the current status of the display as described in the table below:																				
	Bit	Symbol	Description				Comment														
	D7	-					'0'														
	D6	VIPF[2]	DPI Pixel Format (RGB Interface Color Format)				'101' = 16-bits / pixel, '110' = 18-bits / pixel, '111' = 24-bits / pixel, others = not defined														
	D5	VIPF[1]																			
	D4	VIPF[0]																			
	D3	-					0														
	D2	IFPF[2]	DBI Pixel Format (Control Interface Color Format)				'101' = 16-bits / pixel, '110' = 18-bits / pixel, '111' = 24-bits / pixel, others = not defined														
	D1	IFPF[1]																			
	D0	IFPF[0]																			
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>77h</td></tr><tr><td>SW Reset</td><td>No Change</td></tr><tr><td>HW Reset</td><td>77h</td></tr></table>													Status	Default Value	Power On Sequence	77h	SW Reset	No Change	HW Reset	77h
	Status	Default Value																			
	Power On Sequence	77h																			
	SW Reset	No Change																			
	HW Reset	77h																			
Flow Chart	<div><div><p>Serial I/F Mode</p><div><div>RDDCOLMOD (0Ch)</div><div>Send D[7:0]</div></div></div><div><p>Parallel I/F Mode</p><div><div>RDDCOLMOD (0Ch)</div><div>Dummy Read</div><div>Send D[7:0]</div></div></div><div>Host Driver</div></div>																				
	<div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																				

RDDIM (0D00h): Get Display Mode

0D00h				RDDIM (Read Display Image Mode)																	
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
		MIPI	Other																		
RDDIM	R	0Dh	0D00h	x	D7	D6	D5	D4	D3	D2	D1	D0	00								
Description	The display module returns the display image mode status.																				
	Bit	Symbol	Description		Comment																
	D7	Reserved			'0'																
	D6	Reserved			'0'																
	D5	INVON	Inversion On/Off		"0" = Inversion is Off "1" = Inversion is On,																
	D4	ALLON	All Pixel On		'0' = Normal display '1' = White display																
	D3	ALLOFF	All Pixel Off		'0' = Normal display '1' = Black display																
	D2~D0	Reserved			'000'																
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>SW Reset</td><td>00h</td></tr><tr><td>HW Reset</td><td>00h</td></tr></table>													Status	Default Value	Power On Sequence	00h	SW Reset	00h	HW Reset	00h
	Status	Default Value																			
	Power On Sequence	00h																			
	SW Reset	00h																			
	HW Reset	00h																			
Flow Chart	<div><div><div>Serial I/F Mode</div><div>RDDIM (0Dh)</div><div>Send D[7:0]</div></div><div><div>Parallel I/F Mode</div><div>RDDIM (0Dh)</div><div>Dummy Read</div><div>Send D[7:0]</div></div><div>Host Driver</div></div> <div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																				

RDDSM (0E00h): Get Signal Mode

0E00h				RDDSM (Read Display Signal Mode)									
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
RDDSM	R	0Eh	0E00h	x	D7	D6	D5	D4	D3	D2	D1	D0	00
Description	The display module returns the Display Signal Mode.												
	Bit	Symbol	Description				Comment						
	D7	TEON	Tearing Effect Line On/Off				"0" = Off "1" = On						
	D6	TELOM	Tearing Effect Line mode				"0" = mode1 "1" = mode2						
	D5	Reserved					'0'						
	D4	Reserved					'0'						
	D3	Reserved					'0'						
	D2	Reserved					'0'						
	D1	Reserved					'0'						
	D0	Error on DSI	Error on DSI				'0' = No Error '1' = Error						
Default													
	Status												Default Value
	Power On Sequence												00h
	SW Reset												00h
	HW Reset												00h
Flow Chart													
	Serial I/F Mode												
	Parallel I/F Mode												
	Host Driver												
Legend													
Command													
Parameter													
Display													
Action													
Mode													
Sequential transfer													

RDDSDR (0F00h): Get Diagnostic Result

0F00H				RDDSDR (Read Display Self-Diagnostic Result)																	
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
		MIPI	Other																		
RDDSDR	R	0Fh	0F00h	x	Register Loading Detection			D3	D2	D1	D0	00									
Description	The display module returns the self-diagnostic results following a Sleep Out command.																				
	Bit	Symbol	Description						Comment												
	D7~D4	RELD	Register Loading Detection																		
	D3	Reserved							'0'												
	D2	Reserved							'0'												
	D1	Reserved							'0'												
	D0	Reserved							'0'												
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>SW Reset</td><td>00h</td></tr><tr><td>HW Reset</td><td>00h</td></tr></table>													Status	Default Value	Power On Sequence	00h	SW Reset	00h	HW Reset	00h
	Status	Default Value																			
	Power On Sequence	00h																			
	SW Reset	00h																			
	HW Reset	00h																			
Flow Chart	<div><div><div>Serial I/F Mode</div><div>RDDSDR (0Fh)</div><div>Send D[7:0]</div></div><div><div>Parallel I/F Mode</div><div>RDDSTR (0Fh)</div><div>Dummy Read</div><div>Send D[7:0]</div></div><div>Host Driver</div></div> <div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																				

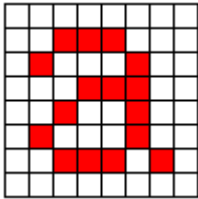
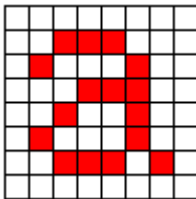
SLPIN (1000h): Enter Sleep mode

1000H		SLPIN (Sleep In)																			
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
		MIPI	Other																		
SLPIN	W	10h	1000h	No Argument																	
Description	<p>This command causes the display module to enter the minimum power consumption mode. In this mode the DC/DC converter is stopped, Internal display oscillator is stopped, and panel scanning is stopped. The control Interface such as registers is still working and keeps its values.</p> <p>After Sleep in command, user can send PCLK, HS and VS information on RGB I/F for blank display and this information is valid during 2 frames if there is used Normal Mode On in Sleep Out-mode.</p> <p>There is used an internal oscillator for blank display.</p>																				
Restriction	<p>This command has no effect when the display module is already in Sleep mode. Sleep In Mode can only be exit by the Sleep Out Command (11h).</p> <p>It must wait 5msec before sending next command for the supply voltages and clock circuits to stabilize.</p> <p>It must wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.</p>																				
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Sleep In Mode</td></tr><tr><td>SW Reset</td><td>Sleep In Mode</td></tr><tr><td>HW Reset</td><td>Sleep In Mode</td></tr></table>													Status	Default Value	Power On Sequence	Sleep In Mode	SW Reset	Sleep In Mode	HW Reset	Sleep In Mode
Status	Default Value																				
Power On Sequence	Sleep In Mode																				
SW Reset	Sleep In Mode																				
HW Reset	Sleep In Mode																				
Flow Chart	<div><div><div>SPLIN (10h)</div><div>Display whole blank screen (Automatic No effect to DISP ON/OFF Command)</div><div>Drain charge from panel</div></div><div><div>Stop DC/DC Converter</div><div>Stop Internal Oscillator</div><div>Sleep In Mode</div></div></div> <div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																				

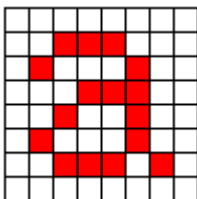
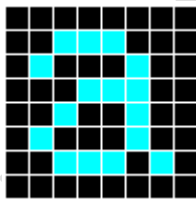
SLPOUT (1100h): Exit Sleep Mode

1100H	SLPOUT (Sleep Out)																				
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
		MIPI	Other																		
SLPOUT	W	11h	1100h	No Argument																	
Description	This command causes the display module to exit Sleep mode. All blocks inside the display module are enabled. The host processor sends PCLK, HS and VS information to display modules two frames before this command is sent when the display module is in Normal Mode.																				
Restriction	This command shall not cause any visible effect on the display device when the display module is not in Sleep mode. The host processor must wait five milliseconds after sending this command before sending another command. This delay allows the supply voltages and clock circuits to stabilize. The host processor must wait 120 milliseconds after sending a Sleep Out command before sending a Sleep-In command. The display module loads the display module's default values to the registers when exiting the Sleep mode. There shall not be any abnormal visual effect on the display device when loading the registers if the factory default and register values are the same or when the display module is not in Sleep mode. The display module runs the self-diagnostic functions after this command is received.																				
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Sleep In Mode</td></tr><tr><td>SW Reset</td><td>Sleep In Mode</td></tr><tr><td>HW Reset</td><td>Sleep In Mode</td></tr></table>													Status	Default Value	Power On Sequence	Sleep In Mode	SW Reset	Sleep In Mode	HW Reset	Sleep In Mode
Status	Default Value																				
Power On Sequence	Sleep In Mode																				
SW Reset	Sleep In Mode																				
HW Reset	Sleep In Mode																				
Flow chart	<div><div><div>SLPOUT (11h)</div><div>Start Internal Oscillator</div><div>Start DC-DC Converter</div><div>Charge Offset voltage for LCD Panel</div></div><div><div>Display whole blank screen for 2 frames (Automatic No effect to DISP ON/OFF Commands)</div><div>Display Image contents in accordance with the current command table settings</div><div>Sleep Out</div></div><div><div>Legend</div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																				

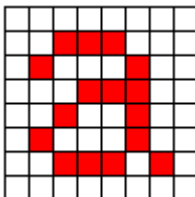
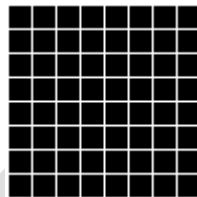
INVOFF (2000H): Exit Invert Mode

2000H		INVOFF (Display Inversion Off)																			
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
		MIPI	Other																		
INVOFF	W	20h	2000h	No Argument																	
Description	This command causes the display module to stop inverting the image data on the display device. No status bits are changed.																				
	<div><div><div>Input Image</div></div><div>→</div><div><div>Display Panel</div></div></div>																				
Restriction	This command has no effect when the display module is not inverting the display image.																				
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display Inversion off</td></tr><tr><td>SW Reset</td><td>Display Inversion off</td></tr><tr><td>HW Reset</td><td>Display Inversion off</td></tr></table>													Status	Default Value	Power On Sequence	Display Inversion off	SW Reset	Display Inversion off	HW Reset	Display Inversion off
Status	Default Value																				
Power On Sequence	Display Inversion off																				
SW Reset	Display Inversion off																				
HW Reset	Display Inversion off																				
Flow Chart	<div><div><div>Display Inversion On Mode</div><div>↓</div><div>INVOFF (20h)</div><div>↓</div><div>Display Inversion OFF Mode</div></div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																				

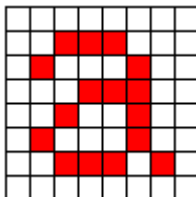
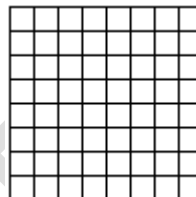
INVON (2100H): Enter Invert Mode

2100H		INVON (Display Inversion On)																			
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
		MIPI	Other																		
INVON	W	21h	2100h	No Argument																	
Description	This command causes the display module to invert the image data only on the display device. No status bits are changed.																				
	<div><div><div>Input Image</div></div><div>→</div><div><div>Display Panel</div></div></div>																				
Restriction	This command has no effect when module is already in inversion on mode.																				
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display Inversion off</td></tr><tr><td>SW Reset</td><td>Display Inversion off</td></tr><tr><td>HW Reset</td><td>Display Inversion off</td></tr></table>													Status	Default Value	Power On Sequence	Display Inversion off	SW Reset	Display Inversion off	HW Reset	Display Inversion off
Status	Default Value																				
Power On Sequence	Display Inversion off																				
SW Reset	Display Inversion off																				
HW Reset	Display Inversion off																				
Flow Chart	<div><div><div>Display Inversion OFF Mode</div><div>↓</div><div>INVON (21h)</div><div>↓</div><div>Display Inversion ON Mode</div></div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																				

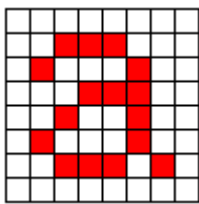
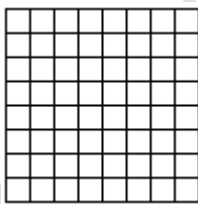
ALLPOFF (2200H): Set All Pixel Off

2200H				ALLPOFF																	
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
		MIPI	Other																		
ALLPOFF	W	22h	2200h	No Argument																	
Description	<p>This command turns the display panel black in Sleep Out mode and a status of the Display On/Off register can be on or off. This command does not change any other status.</p> <div><div><p>Input Image</p></div><div><p>Display Panel</p></div></div> <p>“All Pixels On” or “Normal Display On” commands are used to leave this mode. The display panel is showing the content of the Input Image after “Normal Display On” command.</p>																				
	Restriction -																				
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display Inversion off</td></tr><tr><td>SW Reset</td><td>Display Inversion off</td></tr><tr><td>HW Reset</td><td>Display Inversion off</td></tr></table>													Status	Default Value	Power On Sequence	Display Inversion off	SW Reset	Display Inversion off	HW Reset	Display Inversion off
Status	Default Value																				
Power On Sequence	Display Inversion off																				
SW Reset	Display Inversion off																				
HW Reset	Display Inversion off																				
Flow Chart	<div><div><p>Normal Display ON Mode</p><p>↓</p><p>ALLPOFF (22h)</p><p>↓</p><p>Black Display</p></div><div><p>Legend</p><ul style="list-style-type: none">CommandParameterDisplayActionModeSequential transfer</div></div>																				

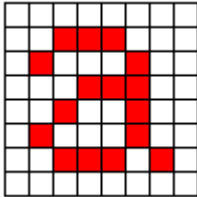
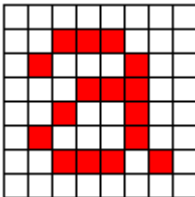
ALLPON (2300H): Set All Pixel On

2300H		ALLPON																			
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
		MIPI	Other																		
ALLPON	W	23h	2300h	No Argument																	
Description	<p>This command turns the display panel white in Sleep Out mode and a status of the Display On/Off register can be on or off. This command does not change any other status.</p> <div><div><p>Input Image</p></div><div><p>Display Panel</p></div></div> <p>“All Pixels Off”, “Normal Display Mode On” commands are used to leave this mode. The display panel is showing the content of the Input Image after “Normal Display On” command.</p>																				
	Restriction -																				
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display Inversion off</td></tr><tr><td>SW Reset</td><td>Display Inversion off</td></tr><tr><td>HW Reset</td><td>Display Inversion off</td></tr></table>													Status	Default Value	Power On Sequence	Display Inversion off	SW Reset	Display Inversion off	HW Reset	Display Inversion off
Status	Default Value																				
Power On Sequence	Display Inversion off																				
SW Reset	Display Inversion off																				
HW Reset	Display Inversion off																				
Flow Chart	<div><div><p>Normal Display ON Mode</p><p>↓</p><p>ALLPON (23h)</p><p>↓</p><p>White Display</p></div><div><p>Legend</p><div><p>Command</p><p>Parameter</p><p>Display</p><p>Action</p><p>Mode</p><p>Sequential transfer</p></div></div></div>																				

DISPOFF (2800h): Set Display Off

2800H				DISPOFF (Display Off)																	
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
		MIPI	Other																		
DISPOFF	W	28h	2800h	No Argument																	
Description	<div><p>This command causes the display module to stop displaying the image data on the display device. No status bits are changed.</p><div><div><p>Input Image</p></div><div><p>→</p><p>(example)</p></div><div><p>Display Panel</p></div></div></div>																				
Restriction	This command has no effect when module is already in display off mode.																				
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display Off</td></tr><tr><td>SW Reset</td><td>Display Off</td></tr><tr><td>HW Reset</td><td>Display Off</td></tr></table>													Status	Default Value	Power On Sequence	Display Off	SW Reset	Display Off	HW Reset	Display Off
Status	Default Value																				
Power On Sequence	Display Off																				
SW Reset	Display Off																				
HW Reset	Display Off																				
Flow Chart	<div><div><div>Display On Mode</div><div>↓</div><div>DISPOFF (28h)</div><div>↓</div><div>Display OFF Mode</div></div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																				

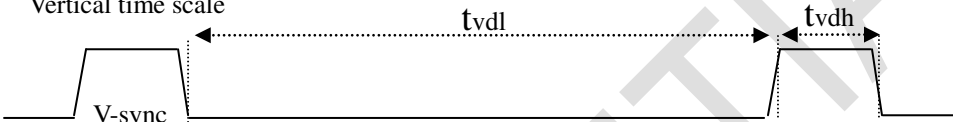
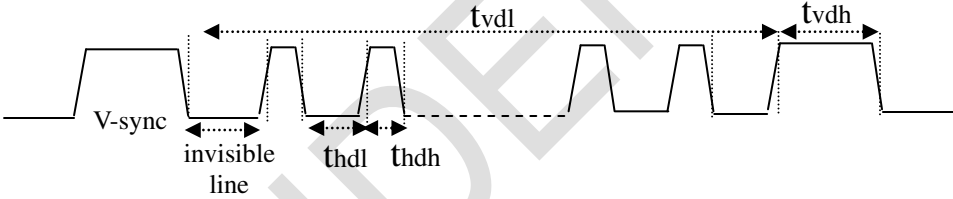
DISPON (2900h): Set Display On

2900H				DISPON (Display On)																	
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
		MIPI	Other																		
DISPON	W	29h	2900h	No Argument																	
Description	<p>This command causes the display module to start displaying the image data on the display device. No status bits are changed.</p> <div><div><p>Input Image</p></div><div><p>→</p><p>(example)</p></div><div><p>Display Panel</p></div></div>																				
Restriction	This command has no effect when module is already in display on mode.																				
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display Off</td></tr><tr><td>SW Reset</td><td>Display Off</td></tr><tr><td>HW Reset</td><td>Display Off</td></tr></table>													Status	Default Value	Power On Sequence	Display Off	SW Reset	Display Off	HW Reset	Display Off
Status	Default Value																				
Power On Sequence	Display Off																				
SW Reset	Display Off																				
HW Reset	Display Off																				
Flow Chart	<div><div><p>Display OFF Mode</p><p>↓</p><p>DISPON (29h)</p><p>↓</p><p>Display ON Mode</p></div><div><p>Legend</p><ul style="list-style-type: none">CommandParameterDisplayActionModeSequential transfer</div></div>																				

TEOFF (3400h): Set Tear OFF

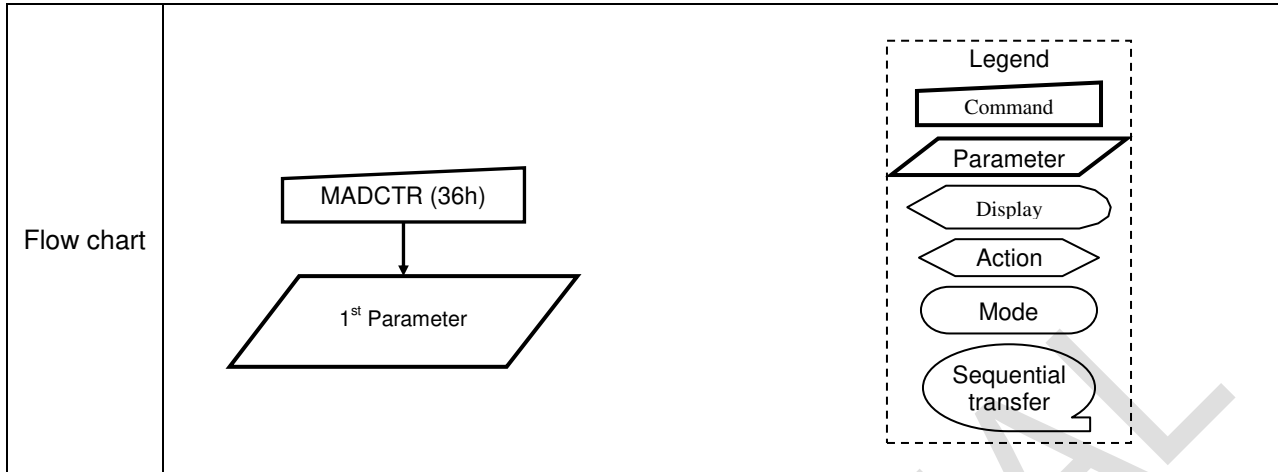
3400H	TEOFF (Tearing Effect Line OFF)																				
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
		MIPI	Other																		
TEOFF	W	34h	3400h	No Argument																	
Description	This command turns off the display module's Tearing Effect output signal from the TE signal line.																				
Restriction	This command has no effect when the Tearing Effect output is already off.																				
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>OFF</td></tr><tr><td>SW Reset</td><td>OFF</td></tr><tr><td>HW Reset</td><td>OFF</td></tr></table>													Status	Default Value	Power On Sequence	OFF	SW Reset	OFF	HW Reset	OFF
Status	Default Value																				
Power On Sequence	OFF																				
SW Reset	OFF																				
HW Reset	OFF																				
Flow Chart	<div><div><div>TE Line Output ON</div><div>↓</div><div>TEOFF (34h)</div><div>↓</div><div>TE Line Output OFF</div></div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																				

TEON (3500h): Set Tear ON

3500H		TEON (Tearing Effect Line ON)																			
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
		MIPI	Other																		
TEON	R/W	35h	3500h	x	0	0	0	0	0	0	0	TELOM	00								
Description	<p>This command turns on the tearing Effect output signal on the TE signal line. The TE signal is not affected by changing MADCTR (36h-D4) (Line Address Order). The Tearing Effect Line On has one parameter that describes the Tearing Effect Output Line mode.</p> <p>If TELOM = 0 The Tearing Effect Output line consists of V-Blanking information only.</p> <p>Vertical time scale</p> 																				
	<p>If TELOM = 1 The Tearing Effect Output line consists of both V-Blanking and H-Blanking information.</p>  <p>The Tearing Effect Output line shall be active low when the display module is in Sleep mode.</p>																				
Restriction	This command has no effect when Tearing Effect output is already ON.																				
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>OFF</td></tr><tr><td>SW Reset</td><td>OFF</td></tr><tr><td>HW Reset</td><td>OFF</td></tr></table>													Status	Default Value	Power On Sequence	OFF	SW Reset	OFF	HW Reset	OFF
Status	Default Value																				
Power On Sequence	OFF																				
SW Reset	OFF																				
HW Reset	OFF																				
Flow Chart	<div><div><div>TE Line Output OFF</div><div>TEON (35h)</div><div>1st Parameter: TELOM</div><div>TE Line Output ON</div></div><div><div>Legend</div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																				

MADCTR (3600h): Set Address Mode

3600H	MADCTR (Scan Direction Control)																																																
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																				
		MIPI	Other																																														
MADCTR	W	36h	3600h	x	D7	D6	D5	D4	D3	D2	D1	D0	00																																				
Description	<p>This command defines the scan direction of Source and Gate Driver. This command makes no change on the other driver status.</p> <table><tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Comment</th></tr><tr><td>D7</td><td>Reserved</td><td></td><td>0</td></tr><tr><td>D6</td><td>Reserved</td><td></td><td>0</td></tr><tr><td>D5</td><td>Reserved</td><td></td><td>0</td></tr><tr><td>D4</td><td>Reserved</td><td></td><td>0</td></tr><tr><td>D3</td><td>RGB</td><td>RGB/BGR Order</td><td>"0"=RGB '1' =BGR</td></tr><tr><td>D2</td><td>Reserved</td><td></td><td>0</td></tr><tr><td>D1</td><td>Reserved</td><td></td><td>0</td></tr><tr><td>D0</td><td>Reserved</td><td></td><td>0</td></tr></table> <p>• Bit D3 – RGB/BGR order</p> <div><div><p>Input Image</p><div><div>R</div><div>G</div><div>B</div></div></div><div><p>D3 = 0 Sent RGB</p></div><div><p>Display Panel</p><div><div>R</div><div>G</div><div>B</div></div></div></div> <div><div><p>Input Image</p><div><div>R</div><div>G</div><div>B</div></div></div><div><p>D3 = 1 Sent BGR</p></div><div><p>Display Panel</p><div><div>B</div><div>G</div><div>R</div></div></div></div>													Bit	Symbol	Description	Comment	D7	Reserved		0	D6	Reserved		0	D5	Reserved		0	D4	Reserved		0	D3	RGB	RGB/BGR Order	"0"=RGB '1' =BGR	D2	Reserved		0	D1	Reserved		0	D0	Reserved		0
	Bit	Symbol	Description	Comment																																													
	D7	Reserved		0																																													
	D6	Reserved		0																																													
	D5	Reserved		0																																													
	D4	Reserved		0																																													
	D3	RGB	RGB/BGR Order	"0"=RGB '1' =BGR																																													
	D2	Reserved		0																																													
	D1	Reserved		0																																													
	D0	Reserved		0																																													
Restriction	Bit D3 is not applicable while resolution is FHD SPR.																																																
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>SW Reset</td><td>No Change</td></tr><tr><td>HW Reset</td><td>00h</td></tr></table>													Status	Default Value	Power On Sequence	00h	SW Reset	No Change	HW Reset	00h																												
	Status	Default Value																																															
	Power On Sequence	00h																																															
	SW Reset	No Change																																															
HW Reset	00h																																																



IDMOFF (3800h): Exit Idle Mode

3800H	IDMOFF (Idle Mode Off)																				
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
		MIPI	Other																		
IDMOFF	W	38h	3800h	No Argument																	
Description	This command causes the display module to exit Idle mode.																				
Restriction	This command has no effect when the display module is not in Idle mode.																				
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Idle Mode Off</td></tr><tr><td>SW Reset</td><td>Idle Mode Off</td></tr><tr><td>HW Reset</td><td>Idle Mode Off</td></tr></table>													Status	Default Value	Power On Sequence	Idle Mode Off	SW Reset	Idle Mode Off	HW Reset	Idle Mode Off
Status	Default Value																				
Power On Sequence	Idle Mode Off																				
SW Reset	Idle Mode Off																				
HW Reset	Idle Mode Off																				
Flow Chart	<div><div><div>Idle mode ON</div><div>IDMOFF (38h)</div><div>Idle mode OFF</div></div><div><div>Legend</div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																				

IDMON (3900h): Enter_idle_mode

3900H				IDMON																																																																																																																																																																																																																																	
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																																																																																																																																																																								
		MIPI	Other																																																																																																																																																																																																																																		
IDMON	W	39h	3900h	No Argument																																																																																																																																																																																																																																	
Description	<p>This command causes the display module to enter Idle Mode. In Idle Mode, color expression is reduced. Colors are shown on the display device using the MSB of each of the R, G and B color components in the Input Image.</p> <div><div><p>Input Image</p></div><div>→</div><div><p>Display Panel</p></div></div>																																																																																																																																																																																																																																				
	<table><tr><th>Color</th><th>R7</th><th>R6</th><th>R5</th><th>R4</th><th>R3</th><th>R2</th><th>R1</th><th>R0</th><th>G7</th><th>G6</th><th>G5</th><th>G4</th><th>G3</th><th>G2</th><th>G1</th><th>G0</th><th>B7</th><th>B6</th><th>B5</th><th>B4</th><th>B3</th><th>B2</th><th>B1</th></tr><tr><td>Black</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td>Blue</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>1</td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td>Red</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>1</td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td>Magen</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>1</td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td>Green</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>1</td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td>Cyan</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>1</td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td>Yellow</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>1</td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td>White</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>1</td><td></td><td></td><td></td><td></td><td></td><td></td></tr></table>													Color	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	Black																								Blue																	1							Red																	1							Magen																	1							Green																	1							Cyan																	1							Yellow																	1							White																	1						
	Color	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1																																																																																																																																																																																																													
Black																																																																																																																																																																																																																																					
Blue																	1																																																																																																																																																																																																																				
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Yellow																	1																																																																																																																																																																																																																				
White																	1																																																																																																																																																																																																																				
Restriction	This command has no effect when module is already in idle on mode.																																																																																																																																																																																																																																				
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Idle Mode Off</td></tr><tr><td>SW Reset</td><td>Idle Mode Off</td></tr><tr><td>HW Reset</td><td>Idle Mode Off</td></tr></table>													Status	Default Value	Power On Sequence	Idle Mode Off	SW Reset	Idle Mode Off	HW Reset	Idle Mode Off																																																																																																																																																																																																																
Status	Default Value																																																																																																																																																																																																																																				
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SW Reset	Idle Mode Off																																																																																																																																																																																																																																				
HW Reset	Idle Mode Off																																																																																																																																																																																																																																				
Flow Chart	<div><div><p>Idle mode OFF</p><p>IDMON (39h)</p><p>Idle mode ON</p></div><div><p>Legend</p><p>Command</p><p>Parameter</p><p>Display</p><p>Action</p><p>Mode</p><p>Sequential transfer</p></div></div>																																																																																																																																																																																																																																				

COLMOD (3A00h): Set Pixel Format

3A00h				COLMOD (Interface Pixel Format)																																				
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																											
		MIPI	Other																																					
COLMOD	W	3Ah	3A00h	x	-	VIPF[2]	VIPF[1]	VIPF[0]	-	IFPF[2]	IFPF[1]	IFPF[0]	77																											
Description	This command sets the pixel format for the RGB image data used by the interface.																																							
	VIPF[2:0] : DPI Pixel Format Definition.																																							
	IFPF[2:0] : MCU Pixel Format Definition.																																							
	If not used DPI interface, then the corresponding bits in the parameter are ignored.																																							
	<table><tr><th colspan="4">Control Interface Color Format</th><th></th><th></th><th></th></tr><tr><td colspan="4">16bit/pixel (65,536 colors)</td><td>1</td><td>0</td><td>1</td></tr><tr><td colspan="4">18bit/pixel (262,144 colors)</td><td>1</td><td>1</td><td>0</td></tr><tr><td colspan="4">24bit/pixel (16.7M colors)</td><td>1</td><td>1</td><td>1</td></tr></table>													Control Interface Color Format							16bit/pixel (65,536 colors)				1	0	1	18bit/pixel (262,144 colors)				1	1	0	24bit/pixel (16.7M colors)				1	1
Control Interface Color Format																																								
16bit/pixel (65,536 colors)				1	0	1																																		
18bit/pixel (262,144 colors)				1	1	0																																		
24bit/pixel (16.7M colors)				1	1	1																																		
Restriction	-																																							
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>77h</td></tr><tr><td>SW Reset</td><td>No Change</td></tr><tr><td>HW Reset</td><td>77h</td></tr></table>													Status	Default Value	Power On Sequence	77h	SW Reset	No Change	HW Reset	77h																			
	Status	Default Value																																						
	Power On Sequence	77h																																						
	SW Reset	No Change																																						
	HW Reset	77h																																						
Flow chart	Example :																																							
	<div><div>16-bits/Pixel Mode</div><div>↓</div><div>COLMOD (3Ah)</div><div>↓</div><div>1st Parameter (06h)</div><div>↓</div><div>18-bits/Pixel Mode</div></div>																																							
	<div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																																							

STESL(4400h) : Set Tear Scan Line

4400h	STESL (Set_Tear_Scanline)																				
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
		MIPI	Other																		
STESL	W	44h	4400h	x	N[15]	N[14]	N[13]	N[12]	N[11]	N[10]	N[9]	N[8]	00								
			4401h	x	N[7]	N[6]	N[5]	N[4]	N[3]	N[2]	N[1]	N[0]	00								
Description	<p>This command turns on the display Tearing Effect output signal on the TE signal line when the display module reaches line N[15:0]. The TE signal is not affected by changing “Set_Address_Mode” bit D4. The Tearing Effect Line On has one parameter that describes the Tearing Effect Output Line mode.</p> <p>See figure in Mode 3 of “Tearing Effect Output”</p> <p>The Tearing Effect Output line shall be active low when the display module is in Sleep mode.</p>																				
Restriction																					
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>N[15:0]=16'h0000</td></tr><tr><td>SW Reset</td><td>No change</td></tr><tr><td>HW Reset</td><td>N[15:0]=16'h0000</td></tr></table>													Status	Default Value	Power On Sequence	N[15:0]=16'h0000	SW Reset	No change	HW Reset	N[15:0]=16'h0000
Status	Default Value																				
Power On Sequence	N[15:0]=16'h0000																				
SW Reset	No change																				
HW Reset	N[15:0]=16'h0000																				
Flow Chart	<div><div><div>TE output ON or OFF</div><div>Set_Tear_Scanline (44h)</div><div>Send 1st parameter N[15:8]</div><div>Send 2nd parameter N[7:0]</div><div>TE output on the Nth line</div></div><div><div>Legend</div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																				

GSL (4500h) : Get Scan Line

4500h	GSL (Get Scan Line)												
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
GSL	R	45h	4500h	x	N[15]	N[14]	N[13]	N[12]	N[11]	N[10]	N[9]	N[8]	0x
			4501h	x	N[7]	N[6]	N[5]	N[4]	N[3]	N[2]	N[1]	N[0]	xx
Description	The display returns the current scan line, N, used to update the display device. The total number of scan lines on a display device is defined as VSYNC + VBP + VACT + VFP. The first scan line is defined as the first line of V-Sync and is denoted as Line 0. When in Sleep Mode, the value returned by “get scan line” is undefined.												
Restriction	-												
Flow Chart	<div><div><div>Get Scan Line (45h)</div><div>Wait 3us</div><div>Dummy Read</div><div>Send 1st parameter N[15:8]</div><div>Send 2nd parameter N[7:0]</div></div><div><div>Legend</div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>												

DSTBON (4F00h): Set Deep Standby Mode

4F00h	DSTBON(Deep Standby Mode On)																				
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
		MIPI	Other																		
DSTBON	W	4Fh	4F00h	x	0	0	0	0	0	0	0	DSTB	00								
Description	<p>This command is used to enter deep standby mode. DSTB="1", enter deep standby mode.</p> <p>Notes:</p> <ol style="list-style-type: none">1. To exit Deep Standby Mode, set RESX low pulse more than 3 msec to pin RESX.2. If user wants to enter DSTB mode from Normal Display directly, it shall enter sleep-in & display-off mode first, and wait 2 frames or more time for completing power-down sequence, and then execute this command to enter DSTB mode.																				
Restriction																					
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>SW Reset</td><td>00h</td></tr><tr><td>HW Reset</td><td>00h</td></tr></table>													Status	Default Value	Power On Sequence	00h	SW Reset	00h	HW Reset	00h
Status	Default Value																				
Power On Sequence	00h																				
SW Reset	00h																				
HW Reset	00h																				
Flow chart	<div><div><div>DSTBON (4Fh)</div><div>Parameter DSTB=1</div><div>Deep Standby Mode</div></div><div><div>Legend</div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																				

WRDISBV (5100h): Write Display Brightness

5100h				WRDISBV																									
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																
		MIPI	Other																										
WRDISBV	W	51h	5100h	x	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	FF																
Description	This command is used to adjust brightness value. In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.																												
	<table><tr><th>DBV[7:0]</th><th>Amount of light</th></tr><tr><td>00h</td><td>None (0%)</td></tr><tr><td>01h</td><td>2/256</td></tr><tr><td>02h</td><td>3/256</td></tr><tr><td>03h</td><td>4/256</td></tr><tr><td>...</td><td>...</td></tr><tr><td>FEh</td><td>255/256</td></tr><tr><td>FFh</td><td>256/256 (default)</td></tr></table>													DBV[7:0]	Amount of light	00h	None (0%)	01h	2/256	02h	3/256	03h	4/256	FEh	255/256	FFh	256/256 (default)
	DBV[7:0]	Amount of light																											
	00h	None (0%)																											
	01h	2/256																											
	02h	3/256																											
	03h	4/256																											
																											
	FEh	255/256																											
	FFh	256/256 (default)																											
Restriction	The display supplier cannot use this command for tuning																												
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>FFh</td></tr><tr><td>SW Reset</td><td>FFh</td></tr><tr><td>HW Reset</td><td>FFh</td></tr></table>													Status	Default Value	Power On Sequence	FFh	SW Reset	FFh	HW Reset	FFh								
	Status	Default Value																											
	Power On Sequence	FFh																											
	SW Reset	FFh																											
	HW Reset	FFh																											
Flow chart	<div><div><div>WRDISBV (51h)</div><div>Parameter DBV[7:0]</div><div>New Brightness Loaded</div></div><div><div>Legend</div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																												

RDDISBV (5200h): Read Display Brightness

5200h	RDDISBV																				
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
		MIPI	Other																		
RDDISBV	R	52h	5200h	x	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	FF								
Description	This command returns the current brightness value. In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.																				
Restriction																					
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>FFh</td></tr><tr><td>SW Reset</td><td>FFh</td></tr><tr><td>HW Reset</td><td>FFh</td></tr></table>													Status	Default Value	Power On Sequence	FFh	SW Reset	FFh	HW Reset	FFh
Status	Default Value																				
Power On Sequence	FFh																				
SW Reset	FFh																				
HW Reset	FFh																				
Flow Chart	<div><div><div>RDDISBV (52h)</div><div>↓</div><div>Send parameter DBV[7:0]</div></div><div>Host Driver</div></div> <div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																				

WRCTRLD (5300h): Write Control Display

5300h				WRDISBV																	
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
		MIPI	Other																		
WRCTRLD	W	53h	5300h	x	HBM[1:0]		BCTRL	0	DD	0	0	0	20								
Description	This command is used to control OLED brightness.																				
	HBM: High Brightness Mode control																				
	HBM[1:0]		Description																		
	00		Normal mode																		
	01		HBM low																		
	10		HBM mid																		
	11		HBM high																		
	BCTRL: Brightness control																				
	BCTRL		Description																		
	0		OFF, DBV[7:0] = 00h.																		
1		ON, DBV[7:0] are active.																			
	DD: Brightness control with dimming effect																				
	DD		Description																		
	0		Dimming effect is OFF.																		
	1		Dimming effect is ON.																		
Restriction	The display supplier cannot use this command for tuning																				
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>20h</td></tr><tr><td>SW Reset</td><td>20h</td></tr><tr><td>HW Reset</td><td>20h</td></tr></table>													Status	Default Value	Power On Sequence	20h	SW Reset	20h	HW Reset	20h
Status	Default Value																				
Power On Sequence	20h																				
SW Reset	20h																				
HW Reset	20h																				
Flow chart	<div><div><div>WRDISBV (53h)</div><div></div><div>BCTRL, DD</div><div></div><div>New Control Value</div></div><div><div>Legend</div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																				

RDCTRLD (5400h): Read Control Display

5400h	RDISBV												
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
RDCTRLD	R	54h	5400h	x	0	0	BCTRL	0	DD	0	0	0	20
Description	This command is used to “read” the setting status of OLED brightness control.												
	BCTRL: Brightness control												
	BCTRL		Description										
	0		OFF, DBV[7:0] = 00h.										
	1		ON, DBV[7:0] are active.										
Description	DD: Brightness control with dimming effect												
	DD		Description										
	0		Dimming effect is OFF.										
	1		Dimming effect is ON.										
	Restriction	-											
Default													
	Status						Default Value						
	Power On Sequence						20h						
	SW Reset						20h						
	HW Reset						20h						
Flow Chart													

WRRADACL (5500h): Write RAD_ACL Control

5500h				WRRADACL																								
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX															
		MIPI	Other																									
WRACL	W	55h	5500h	x	0	0	0	0	0	0	RAD_ACL1	RAD_ACL0	00															
Description	<div><div>This command is used to control Raydium specific function for ACL (Automatic Current Limit)</div><table><tr><th>RAD_ACL1</th><th>RAD_ACL0</th><th>Description</th></tr><tr><td>0</td><td>0</td><td>RAD_ACL function OFF.</td></tr><tr><td>0</td><td>1</td><td>RAD_ACL function effect Low</td></tr><tr><td>1</td><td>0</td><td>RAD_ACL function effect Mid</td></tr><tr><td>1</td><td>1</td><td>RAD_ACL function effect High</td></tr></table></div>													RAD_ACL1	RAD_ACL0	Description	0	0	RAD_ACL function OFF.	0	1	RAD_ACL function effect Low	1	0	RAD_ACL function effect Mid	1	1	RAD_ACL function effect High
RAD_ACL1	RAD_ACL0	Description																										
0	0	RAD_ACL function OFF.																										
0	1	RAD_ACL function effect Low																										
1	0	RAD_ACL function effect Mid																										
1	1	RAD_ACL function effect High																										
Restriction	The display supplier cannot use this command for tuning																											
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>SW Reset</td><td>00h</td></tr><tr><td>HW Reset</td><td>00h</td></tr></table>													Status	Default Value	Power On Sequence	00h	SW Reset	00h	HW Reset	00h							
Status	Default Value																											
Power On Sequence	00h																											
SW Reset	00h																											
HW Reset	00h																											
Flow chart	<div><div><div>WRRADACL (55h)</div><div>Parameter RAD_ACL[1:0]</div><div>New RAD_ACL control</div></div><div><div>Legend</div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																											

RDRADACL (5600h): Read RAD_ACL Control

5600h	RDRADACL																											
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX															
		MIPI	Other																									
RDACL	R	56h	5600h	x	0	0	0	0	0	0	RAD_ ACL1	RAD_ ACL0	00															
Description	<div><div>This command is used to “Read” status value of Raydium specific function for ACL (Automatic Current Limit)</div><table><tr><th>RAD_ ACL1</th><th>RAD_ ACL0</th><th>Description</th></tr><tr><td>0</td><td>0</td><td>RAD ACL function OFF.</td></tr><tr><td>0</td><td>1</td><td>RAD ACL function effect Low</td></tr><tr><td>1</td><td>0</td><td>RAD ACL function effect Mid</td></tr><tr><td>1</td><td>1</td><td>RAD ACL function effect High</td></tr></table></div>													RAD_ ACL1	RAD_ ACL0	Description	0	0	RAD ACL function OFF.	0	1	RAD ACL function effect Low	1	0	RAD ACL function effect Mid	1	1	RAD ACL function effect High
RAD_ ACL1	RAD_ ACL0	Description																										
0	0	RAD ACL function OFF.																										
0	1	RAD ACL function effect Low																										
1	0	RAD ACL function effect Mid																										
1	1	RAD ACL function effect High																										
Restriction																												
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>SW Reset</td><td>00h</td></tr><tr><td>HW Reset</td><td>00h</td></tr></table>													Status	Default Value	Power On Sequence	00h	SW Reset	00h	HW Reset	00h							
Status	Default Value																											
Power On Sequence	00h																											
SW Reset	00h																											
HW Reset	00h																											
Flow Chart	<div><div><div>RDRADACL (56h)</div><div>Send parameter RAD_ ACL[1:0]</div></div><div>Host Driver</div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																											

WRCE (5800h) : Write CE

5800h	WRCE (Write_Color_Enhancement)												
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
WRCE	W	58h	5800h	x	CTE_EN	CTE_LEVEL_3	CTE_LEVEL_2	CTE_LEVEL_1	CTE_LEVEL_0	CTE_SLR_EN	-	-	48
Description	This command is used to set the parameters for CE (color enhance)												
	Bit		Description				Value						
	CTE_EN		Contrast Enhancement Enable				'0': disable; '1': enable						
	CTE_LEVEL[3:0]		Contrast enhancement Level				0~2, low to high , Manual Mode0 4~6, low to high , Manual Mode1 8~10, low to high , Auto Mode						
	CTE_SLR_EN		Contrast Enhancement Sun-light Eeadable Enable				'0': disable; '1': enable						
Restriction													
Flow Chart	<div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>												

RDCE (5900h) : Read CE

5900h		RDCE (Read_Color_Enhancement)																							
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
		MIPI	Other																						
RDCE	R	59h	5900h	x	CTE_EN	CTE_LEVEL_3	CTE_LEVEL_2	CTE_LEVEL_1	CTE_LEVEL_0	CTE_SLR_EN	-	-	48												
Description	This command is used to read the parameters for CE (color enhance)																								
	<table><tr><th>Bit</th><th>Description</th><th>Value</th></tr><tr><td>CTE_EN</td><td>Contrast Enhancement Enable</td><td>'0' : disable; '1': enable</td></tr><tr><td>CTE_LEVEL[3:0]</td><td>Contrast enhancement Level</td><td>0~2, low to high , Manual Mode0 4~6, low to high , Manual Mode1 8~10 low to high, Auot Mode</td></tr><tr><td>CTE_SLR_EN</td><td>Contrast Enhancement Sun-light Eeadable Enable</td><td>'0' : disable; '1': enable</td></tr></table>													Bit	Description	Value	CTE_EN	Contrast Enhancement Enable	'0' : disable; '1': enable	CTE_LEVEL[3:0]	Contrast enhancement Level	0~2, low to high , Manual Mode0 4~6, low to high , Manual Mode1 8~10 low to high, Auot Mode	CTE_SLR_EN	Contrast Enhancement Sun-light Eeadable Enable	'0' : disable; '1': enable
	Bit	Description	Value																						
	CTE_EN	Contrast Enhancement Enable	'0' : disable; '1': enable																						
	CTE_LEVEL[3:0]	Contrast enhancement Level	0~2, low to high , Manual Mode0 4~6, low to high , Manual Mode1 8~10 low to high, Auot Mode																						
CTE_SLR_EN	Contrast Enhancement Sun-light Eeadable Enable	'0' : disable; '1': enable																							
Restriction																									
Flow Chart	<div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																								

WRCE1 (5A00h) : Write CE1

5A00h	WRCE1 (Set_Color_Enhancement_1)												
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
WRCE1	W	5Ah	5A00h	x	SKIN_EN	X	SKIN_LEVEL [1]	SKIN_LEVEL [0]	EN_VIVID_ENH	X	CE_LEVEL [1]	CE_LEVEL [0]	11
Description	This command is used to set the parameters for CE (color enhance)												
	Bit		Description						Value				
	SKIN_EN		Skin Color enable						'0' : disable; '1': enable				
	SKIN_LEVEL[1:0]		Skin Color level						0~2, low to high				
	EN_VIVID_ENH		Vivid Color enable						'0' : disable; '1': enable				
		CE_LEVEL[1:0]		Vivid Color Level						0~2, low to high			
Restriction													
Flow Chart	<div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>												

RDCE1 (5B00h) : Read CE1

5B00h	RDCE1 (Read_Color_Enhancement_1)																											
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX															
		MIPI	Other																									
RDCE1	R	5Ah	5A00h	x	SKIN_EN	X	SKIN_LEVEL [1]	SKIN_LEVEL [0]	EN_VIVID_ENH	X	CE_LEVEL [1]	CE_LEVEL [0]	11															
Description	This command is used to read the parameters for CE (color enhance)																											
	<table><tr><th>Bit</th><th>Description</th><th>Value</th></tr><tr><td>SKIN_EN</td><td>Skin Color enable</td><td>'0' : disable; '1': enable</td></tr><tr><td>SKIN_LEVEL[1:0]</td><td>Skin Color level</td><td>0~2, low to high</td></tr><tr><td>EN_VIVID_ENH</td><td>Vivid Color enable</td><td>'0' : disable; '1': enable</td></tr><tr><td>CE_LEVEL[1:0]</td><td>Vivid Color Level</td><td>0~2, low to high</td></tr></table>													Bit	Description	Value	SKIN_EN	Skin Color enable	'0' : disable; '1': enable	SKIN_LEVEL[1:0]	Skin Color level	0~2, low to high	EN_VIVID_ENH	Vivid Color enable	'0' : disable; '1': enable	CE_LEVEL[1:0]	Vivid Color Level	0~2, low to high
	Bit	Description	Value																									
	SKIN_EN	Skin Color enable	'0' : disable; '1': enable																									
	SKIN_LEVEL[1:0]	Skin Color level	0~2, low to high																									
EN_VIVID_ENH	Vivid Color enable	'0' : disable; '1': enable																										
CE_LEVEL[1:0]	Vivid Color Level	0~2, low to high																										
Restriction																												
Flow Chart	<div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																											

WRCE2 (5C00h) : Write CE2

5C00h	WRCE2 (Set_Color_Enhancement_2)																											
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX															
		MIPI	Other																									
WRCE2	W	5Ch	5C00h	x	SLR_EN	-	SLR_LEVEL[1]	SLR_LEVEL[0]	EN_EDGE_ENH	EN_EDGE_LEVEL[2]	EN_EDGE_LEVEL[1]	EN_EDGE_LEVEL[0]	14															
Description	This command is used to set the parameters for CE (color enhance)																											
	<table><tr><th>Bit</th><th>Description</th><th>Value</th></tr><tr><td>SLR_EN</td><td>Sunlight Readable Enhancement enable</td><td>0 : disable 1 : enable</td></tr><tr><td>SLR_LEVEL[1:0]</td><td>Sunlight Readable Enhancement level</td><td>0~2, low to high</td></tr><tr><td>EN_EDGE_ENH</td><td>Edge enhancement enable</td><td>0 : disable 1 : enable</td></tr><tr><td>EDGE_LEVEL[2:0]</td><td>Edge enhancement Level</td><td>0~2, low to high</td></tr></table>													Bit	Description	Value	SLR_EN	Sunlight Readable Enhancement enable	0 : disable 1 : enable	SLR_LEVEL[1:0]	Sunlight Readable Enhancement level	0~2, low to high	EN_EDGE_ENH	Edge enhancement enable	0 : disable 1 : enable	EDGE_LEVEL[2:0]	Edge enhancement Level	0~2, low to high
	Bit	Description	Value																									
	SLR_EN	Sunlight Readable Enhancement enable	0 : disable 1 : enable																									
	SLR_LEVEL[1:0]	Sunlight Readable Enhancement level	0~2, low to high																									
	EN_EDGE_ENH	Edge enhancement enable	0 : disable 1 : enable																									
EDGE_LEVEL[2:0]	Edge enhancement Level	0~2, low to high																										
Restriction	-																											
Flow Chart	<div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																											

RDCE2 (5D00h) : Read CE2

5D00h	RDCE2 (Set_Color_Enhancement_2)																											
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX															
		MIPI	Other																									
RDCE2	R	5Dh	5D00h	x	SLR_EN	-	SLR_LEVEL[1]	SLR_LEVEL[0]	EN_EDGE_ENH	EN_EDGE_LEVEL[2]	EN_EDGE_LEVEL[1]	EN_EDGE_LEVEL[0]	14															
Description	This command is used to read the parameters for CE (color enhance)																											
	<table><tr><th>Bit</th><th>Description</th><th>Value</th></tr><tr><td>SLR_EN</td><td>Sunlight Readable Enhancement enable</td><td>0 : disable 1 : enable</td></tr><tr><td>SLR_LEVEL[1:0]</td><td>Sunlight Readable Enhancement level</td><td>0~2, low to high</td></tr><tr><td>EN_EDGE_ENH</td><td>Edge enhancement enable</td><td>0 : disable 1 : enable</td></tr><tr><td>EDGE_LEVEL[2:0]</td><td>Edge enhancement Level</td><td>0~2, low to high</td></tr></table>													Bit	Description	Value	SLR_EN	Sunlight Readable Enhancement enable	0 : disable 1 : enable	SLR_LEVEL[1:0]	Sunlight Readable Enhancement level	0~2, low to high	EN_EDGE_ENH	Edge enhancement enable	0 : disable 1 : enable	EDGE_LEVEL[2:0]	Edge enhancement Level	0~2, low to high
	Bit	Description	Value																									
	SLR_EN	Sunlight Readable Enhancement enable	0 : disable 1 : enable																									
	SLR_LEVEL[1:0]	Sunlight Readable Enhancement level	0~2, low to high																									
	EN_EDGE_ENH	Edge enhancement enable	0 : disable 1 : enable																									
EDGE_LEVEL[2:0]	Edge enhancement Level	0~2, low to high																										
Restriction																												
Flow Chart	<div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																											

WRTMR (6200h) : Write CE3 (temper)

6200h	WRTMR (Write_Temper_Level)												
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
WRTMR	W	62h	6200h	x	TEMPER_EN	TEMPER_LEVEL [6]	TEMPER_LEVEL [5]	TEMPER_LEVEL [4]	TEMPER_LEVEL [3]	TEMPER_LEVEL [2]	TEMPER_LEVEL [1]	TEMPER_LEVEL [0]	00
Description	This command is used to set the parameters for CE (color enhance)												
	Bit		Description						Value				
	TEMPER_EN		Temperature enable						0 : disable 1 : enable				
	TEMPER_LEVEL[6:0]		Temperature Set						0~64 setting				
Restriction	-												
Flow Chart	<div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>												

RDTMR (6300h) : Read CE3 (temper)

6300h	RDTMR (Read_Temper_Level)																					
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX									
		MIPI	Other																			
RDTMR	R	63h	6300h	x	TEMPER_EN	TEMPER_LEVEL[6]	TEMPER_LEVEL[5]	TEMPER_LEVEL[4]	TEMPER_LEVEL[3]	TEMPER_LEVEL[2]	TEMPER_LEVEL[1]	TEMPER_LEVEL[0]	00									
Description	This command is used to read the parameters for CE (color enhance)																					
	<table><tr><th>Bit</th><th>Description</th><th>Value</th></tr><tr><td>TEMPER_EN</td><td>Temperature enable</td><td>0 : disable 1 : enable</td></tr><tr><td>TEMPER_LEVEL[6:0]</td><td>Temperature Set</td><td>0~64 setting</td></tr></table>													Bit	Description	Value	TEMPER_EN	Temperature enable	0 : disable 1 : enable	TEMPER_LEVEL[6:0]	Temperature Set	0~64 setting
	Bit	Description	Value																			
TEMPER_EN	Temperature enable	0 : disable 1 : enable																				
TEMPER_LEVEL[6:0]	Temperature Set	0~64 setting																				
Restriction																						
Flow Chart	<div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																					

WRPA (6400h) : Write CE4 (Paper)

6400h	WRPA (Write_Paper_Level)												
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
WRPA	W	64h	6400h	x	PAPER_EN	PAPER_LEVEL [6]	PAPER_LEVEL [5]	PAPER_LEVEL [4]	PAPER_LEVEL [3]	PAPER_LEVEL [2]	PAPER_LEVEL [1]	PAPER_LEVEL [0]	00
Description	This command is used to set the parameters for CE (color enhance)												
	Bit		Description							Value			
	PAPER_EN		Paper Mode enable							0 : disable 1 : enable			
	PAPER_LEVEL[6:0]		Paper Mode Set							0~64 setting			
Restriction	-												
Flow Chart	<div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>												

RDPA (6500h) : Read CE4 (Paper)

6500h	RDPA (Read_Paper_Level)																					
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX									
		MIPI	Other																			
RDPA	R	65h	6500h	x	PAPER_EN	PAPER_LEVEL [6]	PAPER_LEVEL [5]	PAPER_LEVEL [4]	PAPER_LEVEL [3]	PAPER_LEVEL [2]	PAPER_LEVEL [1]	PAPER_LEVEL [0]	00									
Description	This command is used to read the parameters for CE (color enhance)																					
	<table><tr><th>Bit</th><th>Description</th><th>Value</th></tr><tr><td>PAPER_EN</td><td>Paper Mode enable</td><td>0 : disable 1 : enable</td></tr><tr><td>PAPER_LEVEL[6:0]</td><td>Paper Mode Set</td><td>0~64 setting</td></tr></table>													Bit	Description	Value	PAPER_EN	Paper Mode enable	0 : disable 1 : enable	PAPER_LEVEL[6:0]	Paper Mode Set	0~64 setting
	Bit	Description	Value																			
PAPER_EN	Paper Mode enable	0 : disable 1 : enable																				
PAPER_LEVEL[6:0]	Paper Mode Set	0~64 setting																				
Restriction																						
Flow Chart	<div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																					

WRWB (6600h) : Write CE5 (WB)

6600h	WRWB (Write_WB_Level)												
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
WRWB	W	66h	6600h	x	WB_EN	WB_LEVEL [6]	WB_LEVEL [5]	WB_LEVEL [4]	WB_LEVEL [3]	WB_LEVEL [2]	WB_LEVEL [1]	WB_LEVEL [0]	00
Description	This command is used to set the parameters for CE (color enhance)												
	Bit		Description						Value				
	WB_EN		White Balance enable						0 : disable 1 : enable				
	WB_LEVEL[6:0]		White Balance Set						0~64 setting				
Restriction	-												
Flow Chart	<div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>												

RDWB (6700h) : Read CE5 (WB)

6700h	RDWB (Read_WB_Level)																					
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX									
		MIPI	Other																			
RDWB	R	67h	6700h	x	WB_EN	WB_LEVEL [6]	WB_LEVEL [5]	WB_LEVEL [4]	WB_LEVEL [3]	WB_LEVEL [2]	WB_LEVEL [1]	WB_LEVEL [0]	00									
Description	This command is used to read the parameters for CE (color enhance)																					
	<table><tr><th>Bit</th><th>Description</th><th>Value</th></tr><tr><td>WB_EN</td><td>White Balance enable</td><td>0 : disable 1 : enable</td></tr><tr><td>WB_LEVEL[6:0]</td><td>White Balance Set</td><td>0~64 setting</td></tr></table>													Bit	Description	Value	WB_EN	White Balance enable	0 : disable 1 : enable	WB_LEVEL[6:0]	White Balance Set	0~64 setting
	Bit	Description	Value																			
WB_EN	White Balance enable	0 : disable 1 : enable																				
WB_LEVEL[6:0]	White Balance Set	0~64 setting																				
Restriction																						
Flow Chart	<div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																					

WRCEMODE (6800h) : Write CE6 (CE Mode)

6800h	WRCEMODE (Write_CE_Mode)																	
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX					
		MIPI	Other															
WRCEMODE	W	68h	6800h	x	-	-	-	-	-	CE_MODE [2]	CE_MODE [1]	CE_MODE [0]	00					
Description	This command is used to set the parameters for CE (color enhance)																	
	<table><tr><th>Bit</th><th>Description</th><th>Value</th></tr><tr><td>CE_MODE[2:0]</td><td>CE Gamut Mode</td><td>1: decrease gamut Mode1 2: decrease gamut Mode2 4: decrease gamut Mode3 others: increase gamut Mode</td></tr></table>													Bit	Description	Value	CE_MODE[2:0]	CE Gamut Mode
Bit	Description	Value																
CE_MODE[2:0]	CE Gamut Mode	1: decrease gamut Mode1 2: decrease gamut Mode2 4: decrease gamut Mode3 others: increase gamut Mode																
Restriction	-																	
Flow Chart	<div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																	

RDCEMODE (6900h) : Read CE6 (CE Mode)

6900h	RDCEMODE (Read_CE_Mode)																	
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX					
		MIPI	Other															
RDCEMODE	R	69h	6900h	x	-	-	-	-	-	CE_MODE [2]	CE_MODE [1]	CE_MODE [0]	00					
Description	This command is used to read the parameters for CE (color enhance)																	
	<table><tr><th>Bit</th><th>Description</th><th>Value</th></tr><tr><td>CE_MODE[2:0]</td><td>CE Gamut Mode</td><td>1: decrease gamut Mode1 2: decrease gamut Mode2 4: decrease gamut Mode3 others: increase gamut Mode</td></tr></table>													Bit	Description	Value	CE_MODE[2:0]	CE Gamut Mode
Bit	Description	Value																
CE_MODE[2:0]	CE Gamut Mode	1: decrease gamut Mode1 2: decrease gamut Mode2 4: decrease gamut Mode3 others: increase gamut Mode																
Restriction	-																	
Flow Chart	<div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																	

WRHDR (6A00h) : Write HDR

6A00h	WRHDR												
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
WRHDR	W	6Ah	6A00h	x	HDR_EN	HDR_LEVEL[6:0]							50
Description	This command is used to set the parameters for CE (color enhance)												
	Bit		Description		Value								
	HDR_EN		High Dynamic Range enable		0 : disable 1 : enable								
	HDR_LEVEL[6:0]		High Dynamic Range Level		0~64 setting								
Restriction	-												
Flow Chart	<div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>												

RDCEMODE (6B00h) : Read HDR

6B00h	RDHDR												
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
RDHDR	R	6Bh	6B00h	x	HDR_EN	HDR_LEVEL[6:0]							00
Description	This command is used to read the parameters for CE (color enhance)												
	Bit		Description		Value								
	HDR_EN		High Dynamic Range enable		0 : disable 1 : enable								
	HDR_LEVEL[6:0]		High Dynamic Range Level		0~64 setting								
Restriction													
Flow Chart	<div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>												

RDDDBS(A100h ~ A104h) : Read DDB Start

A1H	RDDDBS(Read_DDB_Start)																										
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX														
		MIPI	Other																								
RDDDBS	R	A1h	A100h	x	SID[15]	SID[14]	SID[13]	SID[12]	SID[11]	SID[10]	SID[9]	SID[8]	00														
			A101h	x	SID[7]	SID[6]	SID[5]	SID[4]	SID[3]	SID[2]	SID[1]	SID[0]	00														
			A102h	x	MID[15]	MID[14]	MID[13]	MID[12]	MID[11]	MID[10]	MID[9]	MID[8]	00														
			A103h	x	MID[7]	MID[6]	MID[5]	MID[4]	MID[3]	MID[2]	MID[1]	MID[0]	00														
			A104h	x	1	1	1	1	1	1	1	1	1	FF													
Description	1 st parameter : Supplier ID code 2 nd parameter : Supplier ID code 3 rd parameter : Module ID 4 th parameter : Module ID 5 th Exit code (FFh).																										
Restriction																											
Default	<table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>After MTP</th><th>Before MTP</th></tr><tr><td>Power On Sequence</td><td>MTP Value</td><td>00h, 00h, 00h, 00h, FFh</td></tr><tr><td>SW Reset</td><td>MTP Value</td><td>00h, 00h, 00h, 00h, FFh</td></tr><tr><td>HW Reset</td><td>MTP Value</td><td>00h, 00h, 00h, 00h, FFh</td></tr></table>													Status	Default Value		After MTP	Before MTP	Power On Sequence	MTP Value	00h, 00h, 00h, 00h, FFh	SW Reset	MTP Value	00h, 00h, 00h, 00h, FFh	HW Reset	MTP Value	00h, 00h, 00h, 00h, FFh
Status	Default Value																										
	After MTP	Before MTP																									
Power On Sequence	MTP Value	00h, 00h, 00h, 00h, FFh																									
SW Reset	MTP Value	00h, 00h, 00h, 00h, FFh																									
HW Reset	MTP Value	00h, 00h, 00h, 00h, FFh																									
Flow Chart	<div><div><div>Serial I/F Mode</div><div><div>RDDDBS (A1h)</div><div>Dummy Clock</div><div>Send ID1[15:8]</div><div>Send ID1[7:0]</div><div>Send ID2[15:8]</div><div>Send ID2[7:0]</div><div>Send FFh</div></div></div><div><div>Parallel I/F Mode</div><div><div>RDDDBS (A1h)</div><div>Dummy Read</div><div>Send ID1[15:8]</div><div>Send ID1[7:0]</div><div>Send ID2[15:8]</div><div>Send ID2[7:0]</div><div>Send FFh</div></div></div><div><div>Host Driver</div></div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																										

RDDDBC(A800h ~ A804h) : Read DDB Continue

A8	RDDDBC																										
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX														
		MIPI	Other																								
RDDDBC	R	A8h	A800h	x	SID[15]	SID[14]	SID[13]	SID[12]	SID[11]	SID[10]	SID[9]	SID[8]	00														
			A801h	x	SID[7]	SID[6]	SID[5]	SID[4]	SID[3]	SID[2]	SID[1]	SID[0]	00														
			A802h	x	MID[15]	MID[14]	MID[13]	MID[12]	MID[11]	MID[10]	MID[9]	MID[8]	00														
			A803h	x	MID[7]	MID[6]	MID[5]	MID[4]	MID[3]	MID[2]	MID[1]	MID[0]	00														
			A804h	x	1	1	1	1	1	1	1	1	1	FF													
Description	<p>This command returns the supplier identification and display module mode/revision information from the point where RDDDBS command was interrupted by an other command.</p> <p><i>Note: Parameter 0xFF is an “Exit Code”, this means that there is no more data in the DDB block.</i></p> <p><i>Note: For use example,</i></p> <ol style="list-style-type: none">1. Set maximum return packet size=32. Read 0xA1, return 3 bytes SID[7:0], SID[15:8], MID[7:0]3. Read 0xA8, return 2 bytes MID[15:8],RID[7:0], RID[15:8] and 0xFF																										
Restriction	A Read DDB Start command (RDDDBS) should be executed at least once before a Read DDB Continue command (RDDDBC) to define the read location. Otherwise, data read with a Read DDB Continue command is undefined.																										
Default	<table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>After MTP</th><th>Before MTP</th></tr><tr><td>Power On Sequence</td><td>MTP Value</td><td>00h, 00h, 00h, 00h, FFh</td></tr><tr><td>SW Reset</td><td>MTP Value</td><td>00h, 00h, 00h, 00h, FFh</td></tr><tr><td>HW Reset</td><td>MTP Value</td><td>00h, 00h, 00h, 00h, FFh</td></tr></table>													Status	Default Value		After MTP	Before MTP	Power On Sequence	MTP Value	00h, 00h, 00h, 00h, FFh	SW Reset	MTP Value	00h, 00h, 00h, 00h, FFh	HW Reset	MTP Value	00h, 00h, 00h, 00h, FFh
Status	Default Value																										
	After MTP	Before MTP																									
Power On Sequence	MTP Value	00h, 00h, 00h, 00h, FFh																									
SW Reset	MTP Value	00h, 00h, 00h, 00h, FFh																									
HW Reset	MTP Value	00h, 00h, 00h, 00h, FFh																									
Flow Chart	<div><div><div>RDDDBC (A8h)</div><div></div><div>RDDDBS Data D1[7:0], D2[7:0], ... Dn[7:0]</div></div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																										

RDFCS(AA00h) : Read First Checksum

AA00H	RDFCS																				
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
		MIPI	Other																		
RDFCS	R	AAh	AA00h	x	FCS7	FCS6	FCS5	FCS4	FCS3	FCS2	FCS1	FCS0	00								
Description	This command returns the first checksum what has been calculated from “User Command Set” area registers (not include “Manufacture Command Set”) and the frame memory after the write access to those registers and/or frame memory has been done.																				
Restriction	It will be necessary to wait 150ms after there is the last write access on “User Command Set” area registers before there can read this checksum value.																				
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>S/W Reset</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table>													Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h
Status	Default Value																				
Power On Sequence	00h																				
S/W Reset	00h																				
H/W Reset	00h																				
Flow Chart	<div><div><div>RDFCS (AAh)</div><div>Send Parameter FCS[7:0]</div></div><div><div>Legend</div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																				

RDCCS(AF00h) : Read Continue Checksum

AF00H				RDCCS																	
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
		MIPI	Other																		
RDCCS	R	AFh	AF00h	x	CCS7	CCS6	CCS5	CCS4	CCS3	CCS2	CCS1	CCS0	00								
Description	This command returns the continue checksum what has been calculated continuously after the first checksum has calculated from “User Command Set” area registers and the frame memory after the write access to those registers and/or frame memory has been done.																				
Restriction	It will be necessary to wait 300ms after there is the last write access on “User Command Set” area registers before there can read this checksum value in the first time.																				
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>S/W Reset</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table>													Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h
Status	Default Value																				
Power On Sequence	00h																				
S/W Reset	00h																				
H/W Reset	00h																				
Flow Chart	<div><div><div>RDCCS (AFh)</div><div>Send Parameter CCS[7:0]</div></div><div><div>Legend</div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																				

RDCTRLD1 (DA00h) : Read Control ID1

DA00H				RDCTRLD1																							
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX														
		MIPI	Other																								
RDCTRLD1	R	DAh	DA00h	x	ID1								00														
Description	This read byte identifies Module's manufacture ID																										
Restriction	-																										
Default	<table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>After MTP</th><th>Before MTP</th></tr><tr><td>Power On Sequence</td><td>MTP Value</td><td>00h</td></tr><tr><td>SW Reset</td><td>MTP Value</td><td>00h</td></tr><tr><td>HW Reset</td><td>MTP Value</td><td>00h</td></tr></table>													Status	Default Value		After MTP	Before MTP	Power On Sequence	MTP Value	00h	SW Reset	MTP Value	00h	HW Reset	MTP Value	00h
	Status	Default Value																									
		After MTP	Before MTP																								
	Power On Sequence	MTP Value	00h																								
	SW Reset	MTP Value	00h																								
HW Reset	MTP Value	00h																									
Flow Chart	<div><div><div>RDID1 (DAh)</div><div>Send Parameter RDCTRLD1[7:0]</div></div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																										

Status	Default Value	
	After MTP	Before MTP
Power On Sequence	MTP Value	00h
SW Reset	MTP Value	00h
HW Reset	MTP Value	00h



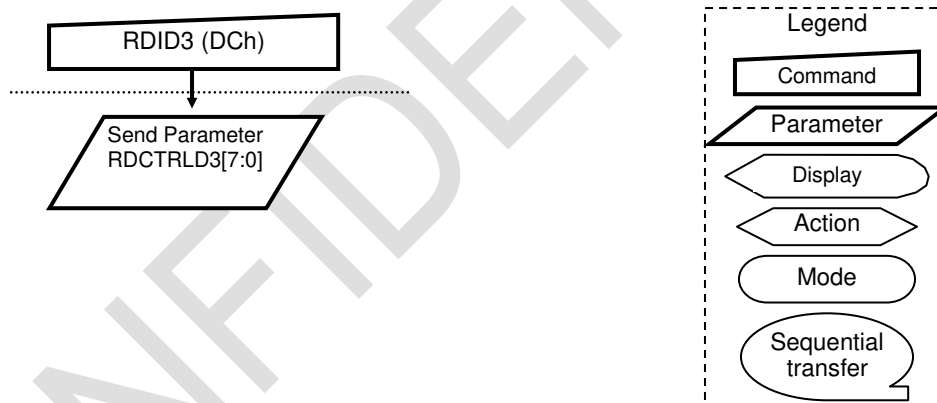
RDCTRLD2 (DB00h) : Read Control ID2

DB00h	RDCTRLD1																										
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX														
		MIPI	Other																								
RDCTRLD2	R	DBh	DB00h	x	ID2								00														
Description	This read byte identifies Module / driver version ID																										
Restriction	-																										
Default	<table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>After MTP</th><th>Before MTP</th></tr><tr><td>Power On Sequence</td><td>MTP Value</td><td>00h</td></tr><tr><td>SW Reset</td><td>MTP Value</td><td>00h</td></tr><tr><td>HW Reset</td><td>MTP Value</td><td>00h</td></tr></table>													Status	Default Value		After MTP	Before MTP	Power On Sequence	MTP Value	00h	SW Reset	MTP Value	00h	HW Reset	MTP Value	00h
	Status	Default Value																									
		After MTP	Before MTP																								
	Power On Sequence	MTP Value	00h																								
	SW Reset	MTP Value	00h																								
HW Reset	MTP Value	00h																									
Flow Chart	<div><div><div>RDID2 (DBh)</div><div>Send Parameter RDCTRLD2[7:0]</div></div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																										

RDCTRLD3 (DC00h) : Read Control ID3

DC00h	RDCTRLD1																										
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX														
		MIPI	Other																								
RDCTRLD3	R	DCh	DC00h	x	ID3								00														
Description	This read byte identifies Module / driver ID																										
Restriction	-																										
Default	<table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>After MTP</th><th>Before MTP</th></tr><tr><td>Power On Sequence</td><td>MTP Value</td><td>00h</td></tr><tr><td>SW Reset</td><td>MTP Value</td><td>00h</td></tr><tr><td>HW Reset</td><td>MTP Value</td><td>00h</td></tr></table>													Status	Default Value		After MTP	Before MTP	Power On Sequence	MTP Value	00h	SW Reset	MTP Value	00h	HW Reset	MTP Value	00h
	Status	Default Value																									
		After MTP	Before MTP																								
	Power On Sequence	MTP Value	00h																								
	SW Reset	MTP Value	00h																								
HW Reset	MTP Value	00h																									
Flow Chart	<div><div><div>RDID3 (DCh)</div><div>Send Parameter RDCTRLD3[7:0]</div></div><div><div>Legend</div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																										

Status	Default Value	
	After MTP	Before MTP
Power On Sequence	MTP Value	00h
SW Reset	MTP Value	00h
HW Reset	MTP Value	00h

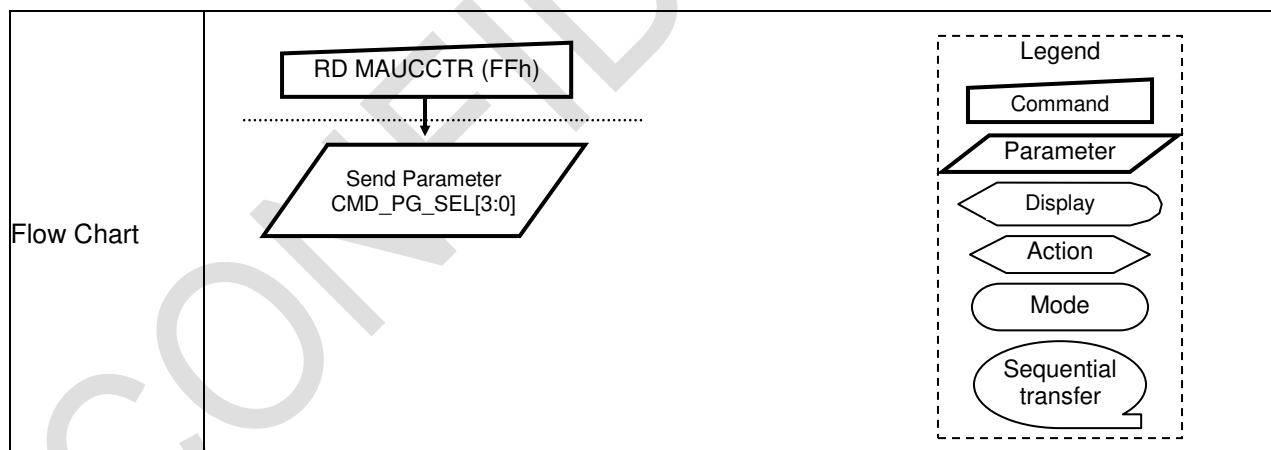


(FE00h) WRMAUCCTR : Write CMD Page Switch

FE00H		WR MAUCCTR (Manufacture Command Set Control)																				
Instruction	R/W	Address		Parameter																		
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX									
CMD Mode Switch	W/R	FEh	FE00h	00h	0	0	0	0	CMD_PG_SEL[3:0]				00									
Description	This command is used to switch the Manufacture Command Pages and User Commands sets.																					
	CMD_PG_SEL [3:0]		Hex Value		Description																	
	0000		00h (default)		User Command Set (UCS = CMD1)																	
	0001		01h		Manufacture Command Set Page0 (CMD2 P0)																	
	0010		02h		Manufacture Command Set Page1 (CMD2 P1)																	
	0011		03h		Manufacture Command Set Page2 (CMD2 P2)																	
	0100		04h		Manufacture Command Set Page3 (CMD2 P3)																	
	0101		05h		Manufacture Command Set Page4 (CMD2 P4)																	
Restriction	-																					
Default	<table><tr><th rowspan="2">Status</th><th>Default Value</th></tr><tr><th>FEh / FE00h</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>S/W Reset</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table>													Status	Default Value	FEh / FE00h	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h
	Status	Default Value																				
		FEh / FE00h																				
	Power On Sequence	00h																				
	S/W Reset	00h																				
H/W Reset	00h																					
Flow Chart	<div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																					

(FF00h) RDMAUCCTR : Read CMD Page

FF00H		RD MAUCCTR (Manufacture Command Set Control)																				
Instruction	R/W	Address		Parameter																		
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX									
RD CMD Status	R	FFh	FF00h	00h	0	0	0	0	CMD_PG_SEL[3:0]				00									
Description	This command is used to switch the Manufacture Command Pages and User Commands sets.																					
	CMD_PG_SEL[3:0]			Hex Value		Description																
	0000			00h (default)		User Command Set (UCS = CMD1)																
	0001			01h		Manufacture Command Set Page0 (CMD2 P0)																
	0010			02h		Manufacture Command Set Page1 (CMD2 P1)																
	0011			03h		Manufacture Command Set Page2 (CMD2 P2)																
	0100			04h		Manufacture Command Set Page3 (CMD2 P3)																
	0101			05h		Manufacture Command Set Page4 (CMD2 P4)																
Restriction	-																					
Default	<table><tr><th rowspan="2">Status</th><th>Default Value</th></tr><tr><th>FFh / FF00h</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>S/W Reset</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table>													Status	Default Value	FFh / FF00h	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h
	Status	Default Value																				
		FFh / FF00h																				
	Power On Sequence	00h																				
	S/W Reset	00h																				
	H/W Reset	00h																				



7. Electrical Characteristics

7.1 Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When RM67295 is used out of the absolute maximum ratings, the RM67295 may be permanently damaged. To use the RM67295 within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the RM67295 will malfunction and cause poor reliability.

item	Symbol	Value	Unit
Power supply voltage	VDDI	-0.3 ~ 5.5	V
Power supply voltage	VDDA, VDDDB, VDDR, VDDAM VCC	-0.3 ~ 5.5	V
Supply voltage (MV)	AVDD-AVSS	-0.3 ~ 6.6	V
	AVEE-AVSS	-0.3 ~ -6.6	V
Supply voltage (HV)	VGHR - VGLR	-0.3 ~ 33	V
Input voltage	VIN	-0.3 ~ VDDI+ 0.3	V
Output voltage	VO	-0.3 ~ VDDI+ 0.3	V
Operating temperature	Topr	-40 ~ 85	°C
Storage temperature	Tstg	-55 ~ 125	°C
Notes: If one of the above items exceeds its maximum limitation momentarily, the quality of the product may be degraded. Absolute maximum limitation. Therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the recommend range.			

7.2 ESD Protection Level

Model	Test Condition	Level
Human Body Mode	R = 1.5 K Ω / C = 100 pF	Pass \pm 2KV
Machine Mode	R = 0 ohm / C = 200 pF	Pass \pm 200V

7.3 Latch-Up Protection Level

The device will not latch up at trigger current levels less than \pm 200mA.

7.4 DC Characteristics

7.4.1 Basic Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Related Pins
Analog Power Supply Voltage	VDD	Operation Voltage	2.5	3.3	3.6	V	Note 1
	VCC	Operating Voltage	1.65	1.8	3.6	V	Note 1
I/O pin Power Supply Voltage	VDDI	I/O supply voltage	1.65	1.8	3.3	V	Note 1
Logic High level input voltage	VIH	VDDI = 1.65V ~ 3.3V	0.8* VDDI	-	VDDI	V	Note 2
Logic Low level input voltage	VIL	VDDI = 1.65V ~ 3.3V	0.0	-	0.2* VDDI	V	Note 2
Logic High level Output voltage	VOH	I _{out} = -1 mA	0.8* VDDI	-	VDDI	V	Note 2
Logic Low level Output voltage	VOL	I _{out} = +1 mA	0.0	-	0.2* VDDI	V	Note 2
Logic High level input current (Except MIPI)	IIHD	V _{in} =0~VDDI			1	μA	Note 2
Logic Low level input current (Except MIPI)	IILD	V _{in} =0~VDDI	-1			μA	Note 2
Logic High level input current (MIPI)	IIHD	V _{in} =0~VDDAM			1	μA	Note 2
Logic Low level input current (MIPI)	IILD	V _{in} =0~VDDAM	-1			μA	Note 2
AVDD booster voltage	AVDD		4.5		6.5	V	Note 2
AVEE booster voltage	AVEE		-6.5		-4.5	V	Note 2
VCL booster voltage	VCL		-VDDDB		-1.5	V	Note 2
VGH booster voltage	VGH		AVDD +VDD		3xAVDD	V	Note 2
VGL booster voltage	VGL		AVEE -AVDD		2AVEE -AVDD -VDD	V	Note 2
Voltage difference between VGHR and VGLR	VGHL	VGHR-VGLR			25	V	Note 2
Gamma reference voltage	VGMP		2.0		AVDD-0.5	V	Note 2,3
	VGSP		0.0		3.3	V	Note 2,3
OSC	Fosc		23	25	27	MHz	
Channel deviation voltage	V _{DEV}			5	10	mV	

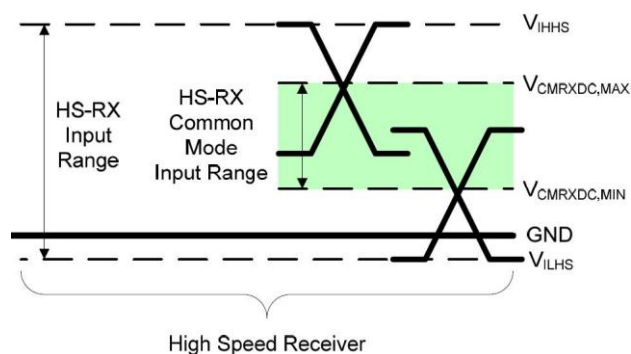
Notes:

1. VDDI=1.65 to 3.3V, VDD=2.5 to 4.8V, VSSI=VSS=DVSS=0V, VDD means VDDA, VDDR, VDDDB. And VSS means VSSA, VSSR, VSSB, AVSS, and VSSAM. VDDDB, VDDA and VDDR should be the same input voltage level and larger than VDDI voltage.
2. TA = -30 to 85 °C
3. AVDD-0.3V >=VGMP > VGSP

7.4.2 MIPI Characteristics

High-Speed Receiver Specification

DC Specifications



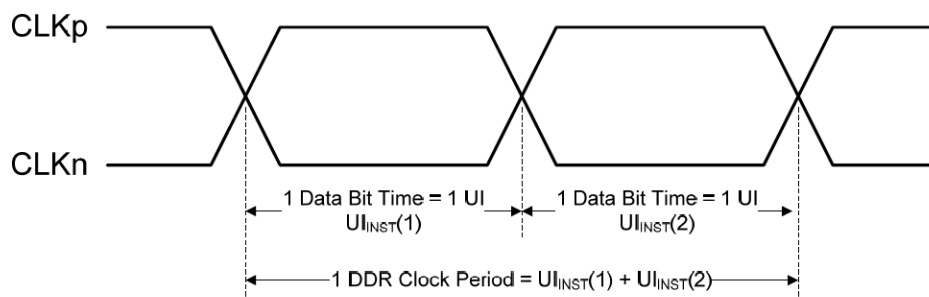
Parameter	Description	Min	Nom	Max	Units	Note
VCMRX(DC)	Common-mode voltage HS receive mode	70		330	mV	1,2
VIDTH	Differential input high threshold			70	mV	
VIDTL	Differential input low threshold	-70			mV	
VIHHS	Single-ended input high voltage			460	mV	1
VILHS	Single-ended input low voltage	-40			mV	1
ZID	Differential input impedance	80	100	125	Ω	

Notes:

1. Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.
2. This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz

Forward high speed transmissions

DDR Clock Definition



Clock Parameter	Symbol	Min	Typ	Max	Units	Notes
UI instantaneous	UI _{INST}	1.00 1.12		12.5 12.5	ns	1,3 2,3

Notes:

1. This value corresponds to a maximum of 1Gbps and a minimum of 80 Mbps data rate for HS Video mode.
2. This value corresponds to a maximum of 900Mbps and a minimum of 80Mbps data rate for HS CMD mode
3. The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.

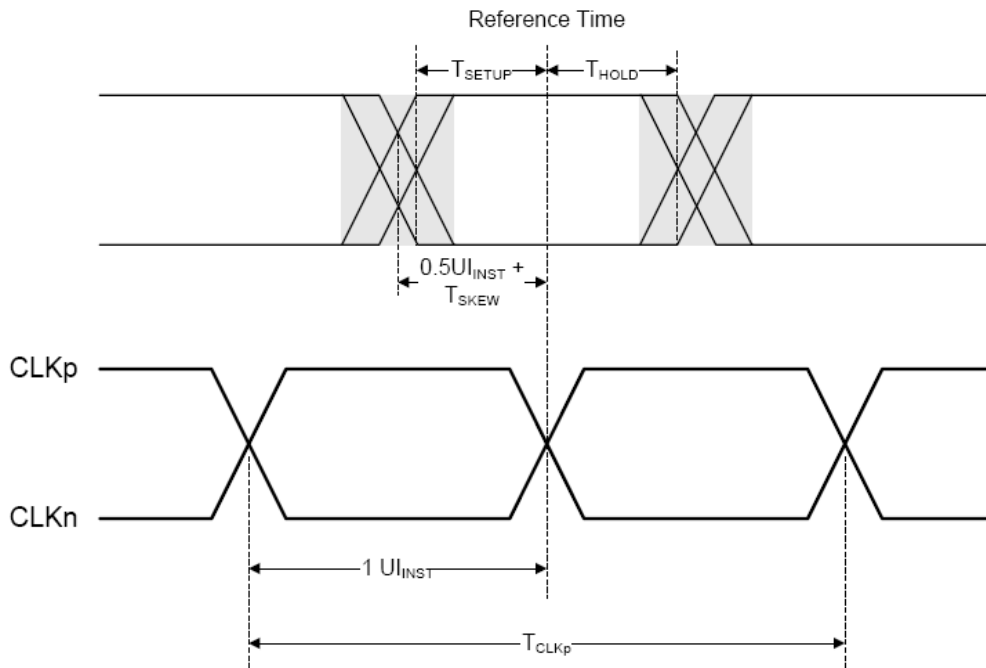
Data-Clock Timing Specifications

Parameter	Symbol	Min	Typ	Max	Units	Notes
Data to Clock Skew [measured at transmitter]	T _{SKEW[TX]}	-0.15		0.15	UI _{INST}	1
Data to Clock Setup Time [receiver]	T _{SETUP[RX]}	0.15			UI _{INST}	2
Clock to Data Hold Time [receiver]	T _{HOLD[RX]}	0.15			UI _{INST}	2

Notes:

1. Total silicon and package delay budget of 0.3*UI_{INST}
2. Total setup and hold window for receiver of 0.3*UI_{INST}. This value may change according to DSI transfer rate.

Data to Clock Timing Definitions



Low power transceiver specifications

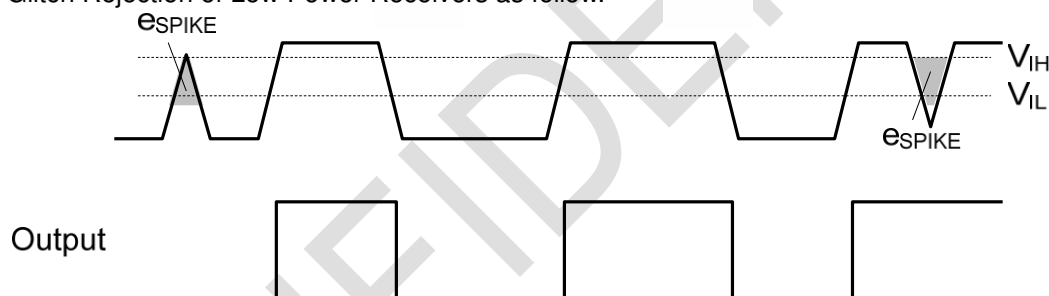
Parameters	Symbol	Condition	Min	Typ	Max	Unit
Logic high level input voltage	VIHCD	Contention Detection (Lane_D0)	450		1350	mV
Logic low level input voltage	VILCD	Contention Detection (Lane_D0)	0		200	mV
Logic high level input voltage	VIH-LPRX	LP-Rx (Lane_CK, Lane_D0, Lane_D1)	880	-	1350	mV
Logic low level input voltage	VIL-LPRX	LP-Rx (Lane_CK, Lane_D0, Lane_D1)	0		550	mV
Logic low level input voltage	VIL-ULPS	LP-Rx ULPS (Lane_CK, Lane_D0, Lane_D1)	0		300	mV
Logic high level input voltage	VOH-LPTX	Contention Detection (Lane_D0)	1.1	1.2	1.3	V
Logic low level input voltage	VOL-LPTX	Contention Detection (Lane_D0)	-50	0	50	mV
eSPIKE ^(1,2,3)	Fig. 2	Input pulse rejection			300	V.ps

Notes:

Time-voltage integration of a spike above VIL when being in LP-0 state or below VIH when being in LP-1 State. An impulse less than this will not change the receiver state.

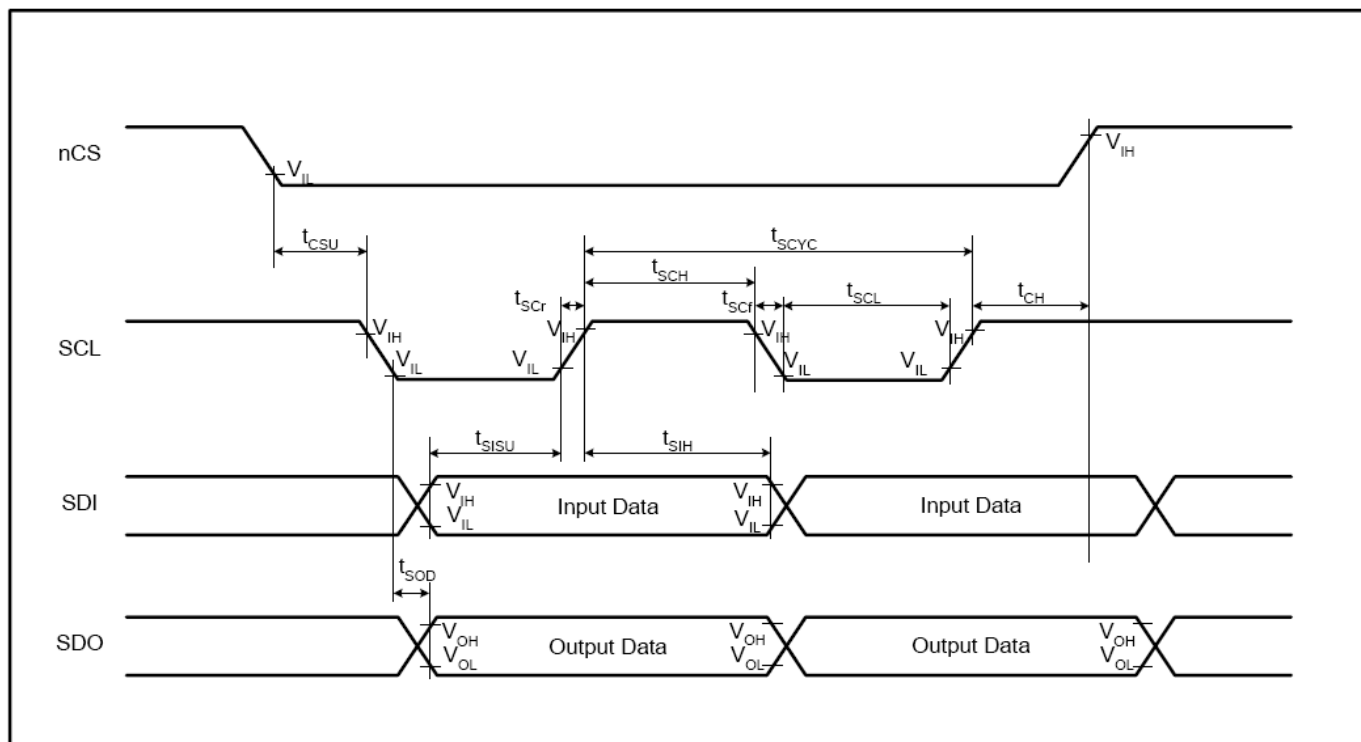
In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.

Input Glitch Rejection of Low Power Receivers as follow.



7.5 AC Characteristics

7.5.1 Serial Interface Characteristics



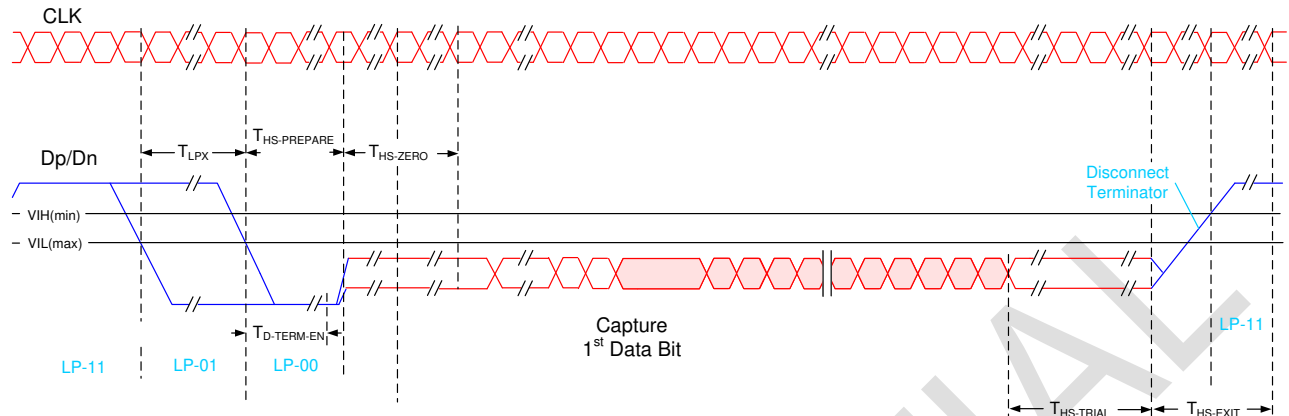
Signal	Symbol	Parameter	MIN	MAX	Unit	Description
SCL	T_{SCYC}	Clock cycle (Write)	100		ns	-
	T_{SCYC}	Clock cycle (Read)	300		ns	
	T_{SCH}	Clock "H" pulse width (Write)	40		ns	
	T_{SCH}	Clock "H" pulse width (Read)	140		ns	
	T_{SCL}	Clock "L" pulse width (Write)	40		ns	
	T_{SCL}	Clock "L" pulse width (Read)	140		ns	
	T_{SCHr}	Clock rise time		5	ns	
	T_{SCHf}	Clock fall time		5	ns	
nCS	T_{CSU}	Chip select setup time	20		ns	-
	T_{CH}	Chip select hold time	50		ns	
SDI	T_{SISU}	Data input setup time	20		ns	-
	T_{SIH}	Data input hold time	20		ns	
SDO	T_{SOD}	Data output setup time		120	ns	-
	T_{SOH}	Data output hold time	5		ns	

Note: Logic high and low levels are specified as 20% and 80% of IOVCC for Input signals.

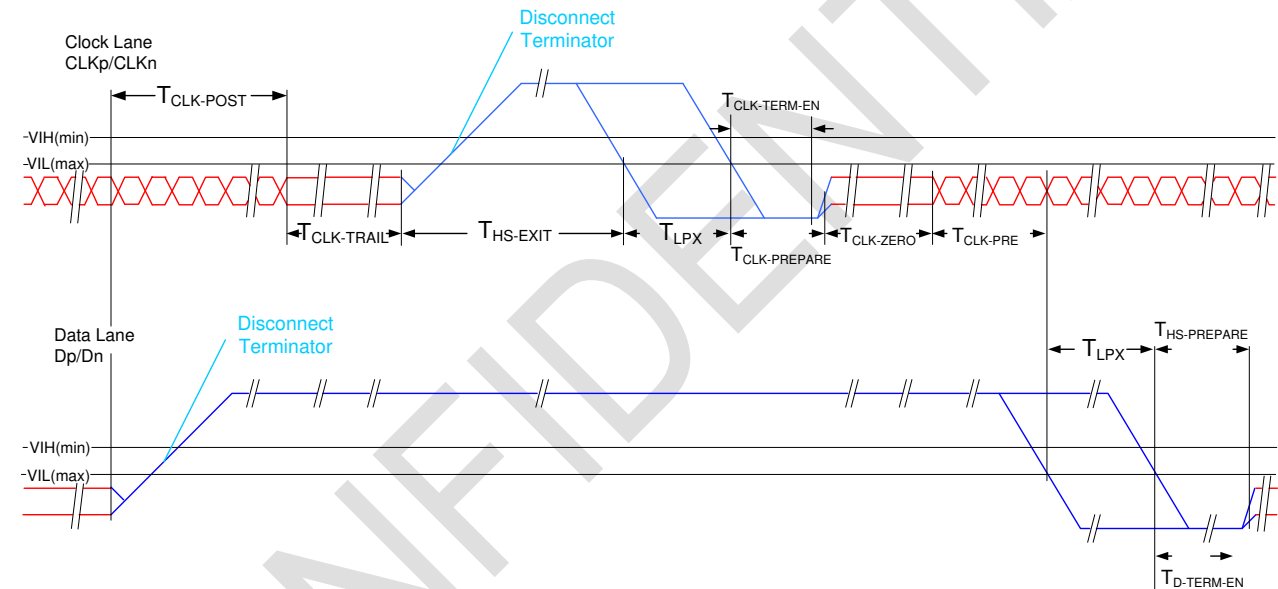
Note: $T_a = -30$ to 70°C , IOVCC=1.65V to 3.3V, VDD=2.5V to 3.6V, GND=0V

7.5.2 DSI Timing Characteristics

HS Data Transmission Burst



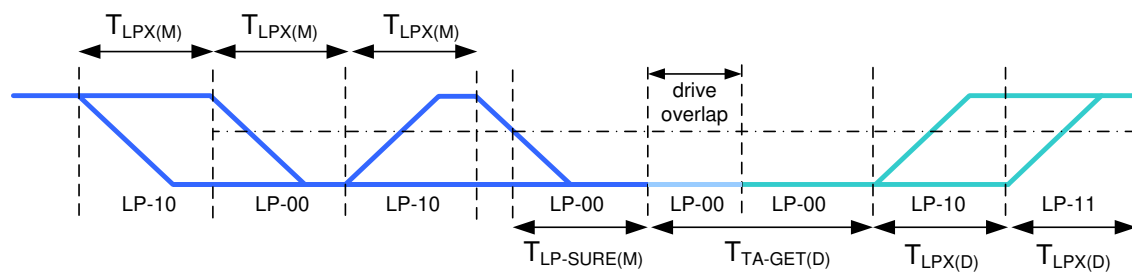
HS clock transmission



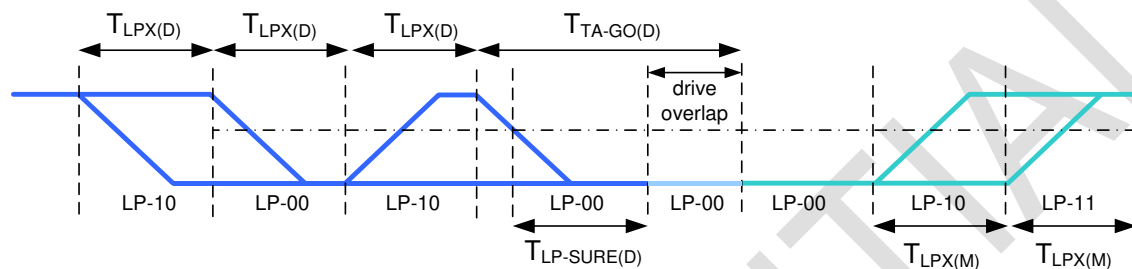
Timing Parameters:

Parameter	Description	Min	Typ	Max	Unit
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$.	$60ns + 52*UI$			ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	300			ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		38	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8			UI
$T_{CLK-PREPARE} + T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		$35 ns + 4*UI$	
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	$40ns + 4*UI$		$85 ns + 6*UI$	ns
$T_{HS-PREPARE} + T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	$145ns + 10*UI$			ns
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	$60ns + 4*UI$			ns

Turnaround Procedure



Bus turnaround (BAT) from MPU to display module timing



Bus turnaround (BAT) from display module to MPU timing

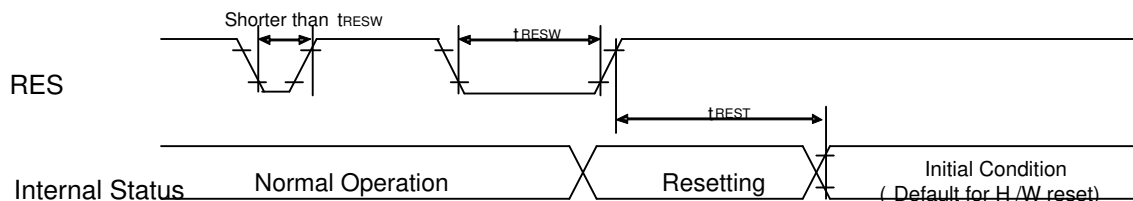
Low Power Mode :

Parameter	Description	Min	Typ	Max	Unit	Notes
$T_{LPX(M)}$	Transmitted length of any Low-Power state period of MCU to display module	50		150	ns	1,2
$T_{TA-SURE(M)}$	Time that the display module waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(M)}$		$2 * T_{LPX(M)}$	ns	2
$T_{LPX(D)}$	Transmitted length of any Low-Power state period of display module to MCU	50		150	ns	1,2
$T_{TA-GET(D)}$	Time that the display module drives the Bridge state (LP-00) after accepting control during a Link Turnaround.		$5 * T_{LPX(D)}$		ns	2
$T_{TA-GO(D)}$	Time that the display module drives the Bridge state (LP-00) before releasing control during a Link Turnaround.		$4 * T_{LPX(D)}$		ns	2
$T_{TA-SURE(D)}$	Time that the MPU waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(D)}$		$2 * T_{LPX(D)}$	ns	2

NOTE:

1. T_{LPX} is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.
2. Transmitter-specific paramete

7.5.3 Reset Timing



Reset input timing:

IOVCC=1.65 to 3.6V, VDD=2.5 to 3.6V, AGND=DGND=0V, Ta=-40 to 85°C

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
t_{RESW}	*1) Reset low pulse width	RESX	10	-	-	-	μs
t_{REST}	*2) Reset complete time	-	-	-	5	When reset applied during Sleep in mode	ms
		-	-	-	120	When reset applied during Sleep out mode	ms

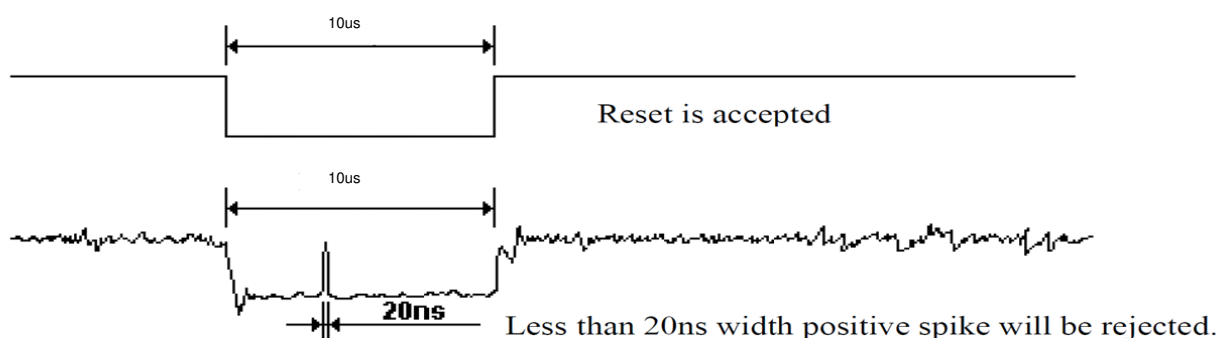
Note 1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5 μs	Reset Rejected
Longer than 10 μs	Reset
Between 5 μs and 10 μs	Reset starts (It depends on voltage and temperature condition.)

Note 2. During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

Note 3. During Reset Complete Time, data in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (t_{REST}) within 5ms after a rising edge of RESX.

Note 4. Spike Rejection also applies during a valid reset pulse as shown below:



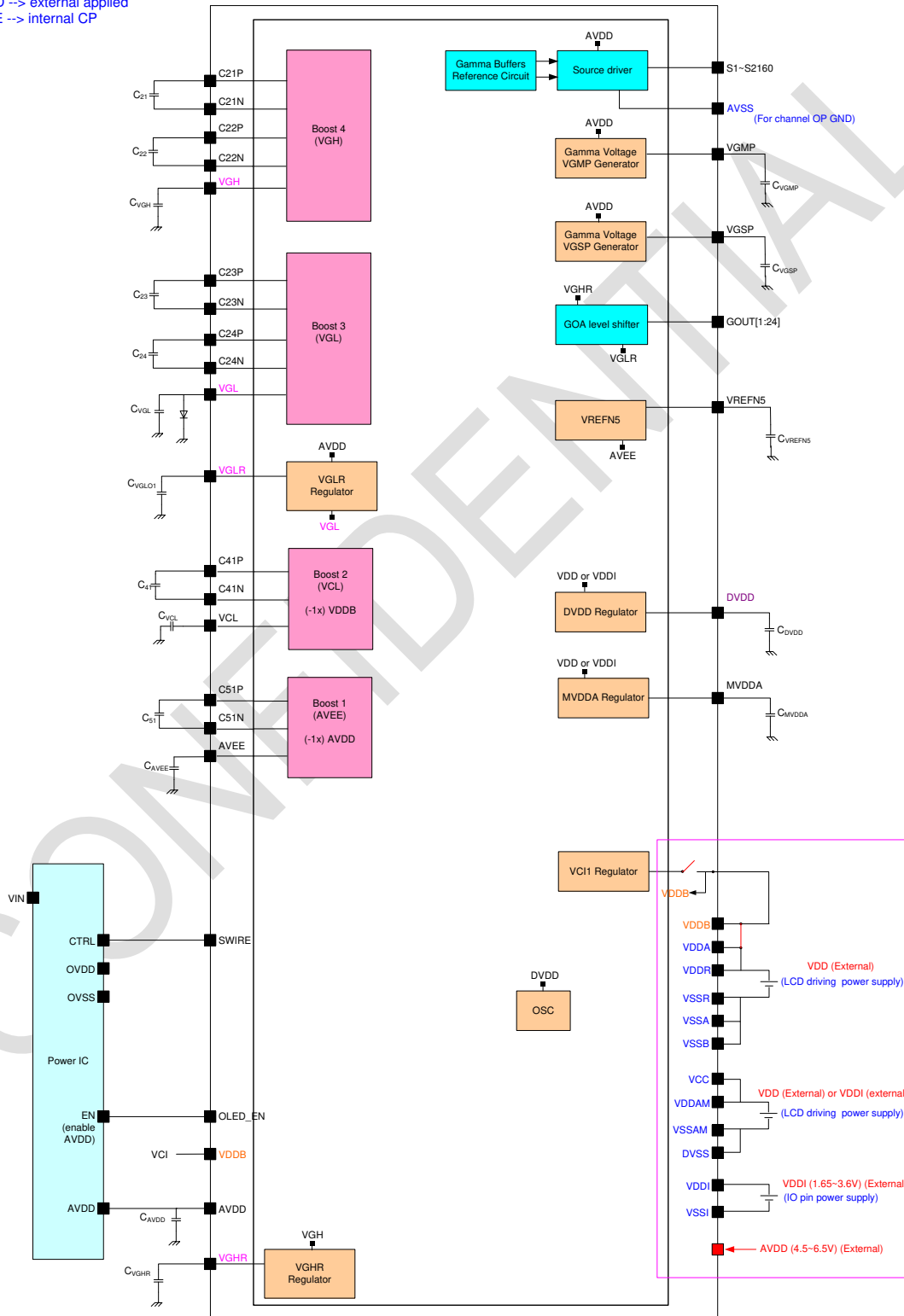
Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

8. Power Generation

8.1 DC/DC Converter Circuit

BSTM = 111

3PWR(VDDI, VCI, AVDD)
VCI=VDDA=VDDB=VDDR
AVDD --> external applied
AVEE --> internal CP



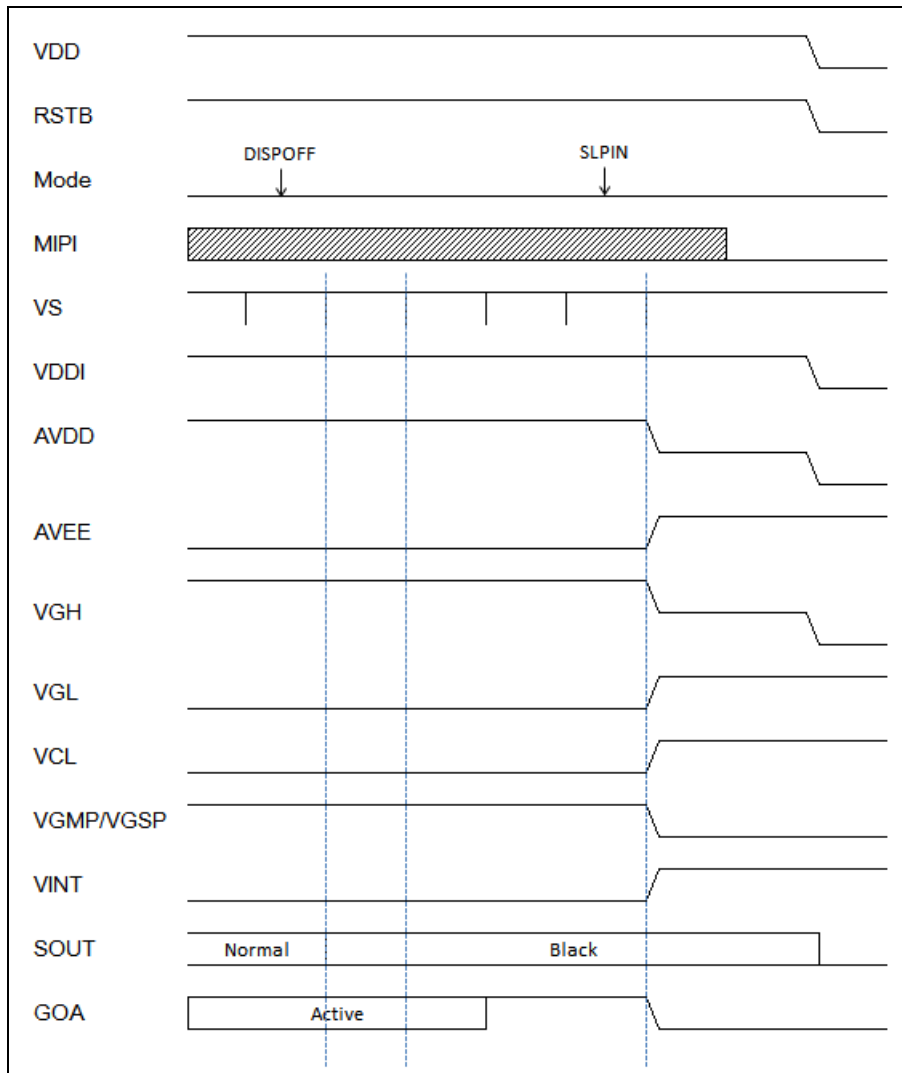
8.3 External Component

No.	Signal Name	Values	Max Ability	Note
1	VDDA, VDDDB, VDDR, VCC	Cap, 4.7uF	6.3V	Analog power input
2	VDDI	Cap, 2.2uF	6.3V	I/O & Digital power input
3	DVDD	Cap, 2.2uF	6.3V	Regulator output
4	MVDDA	Cap, 1uF	6.3V	Regulator output
6	VREFN5	Cap, 2.2uF	6.3V	Regulator output (*Note 1)
7	VGHR	Cap, 2.2uF	16V	Regulator output
8	VGLR	Cap, 2.2uF	16V	Regulator output
9	AVDD	Cap, 4.7uF	10V	AVDD
10	AVEE	Cap, 4.7uF	10V	AVEE
11	C21P/C21N	Cap, 1uF	16V	VGH Pump
12	C22P/C22N	Cap, 1uF	16V	
13	VGH	Cap, 2.2uF	25V	
14	C23P/C23N	Cap, 1uF	16V	VGL Pump
15	C24P/C24N	Cap, 1uF	16V	
16	VGL	Cap, 2.2uF	25V	
17	C41P/C41N	Cap, 1uF	6.3V	VCL Pump
18	VCL	Cap, 2.2uF	6.3V	
19	C51P/C51N	Cap, 1uF	10V	AVEE Pump
20	VGL-GND	Schottky Diode		Prevent from Latch-Up (*Note 2)
21	VGMP	Cap, 1uF	6.3V	Regulator output
22	VGSP	Cap, 1uF	6.3V	Regulator output

Note:

1. The Schottky diode can be removed if the Latch-Up doesn't occur without it. Before testing, it is suggested to keep it.

9.2 Power Off Sequence



9.3 Power Level Modes

Normal display mode on = NORON

Partial mode on = PTLON

Idle mode off = IDMOFF

Idle mode on = IDMON

Sleep out = SLPOUT

Sleep in = SLPIN

Deep standby mode = DSTBON

Definition example:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.

In this mode, the display is able to show maximum 16.7M colors.

2. Partial Mode On, Idle Mode Off, Sleep Out

In this mode, part of the display is used with maximum 16.7M colors.

3. Normal Mode On (full display), Idle Mode On, Sleep Out.

In this mode, the full display is used but with 8 colors.

4. Partial Mode On, Idle Mode On, Sleep Out

In this mode, part of the display is used but with 8 colors.

5. Sleep In Mode.

In this mode, the DC/DC converter, internal oscillator and panel driver circuit are stopped. Only the MPU interface and registers are working with VDDI power supply. Contents of the frame memory can be safe or random.

6. Deep Standby Mode.

In this mode, the DC/DC converter, internal oscillator and panel driver circuit are stopped. The MPU interface and registers are not working. Content of the frame memory is random.

7. Power Off Mode

In this mode, VDDI and VDDA/VDDR/VDDDB are removed.

NOTE:

Transition between mode 1~5 is controllable by MPU commands. Mode 6 is entered for power saving with both power supplies for I/O and analog circuits and can be exited by hardware reset only (RESX=L). Mode 7 is entered only when both power supplies for I/O and analog circuits are removed.

10. Chip Information

- ◆ Chip Thickness= 200um
- ◆ Au Bump:
 1. ILB Size= 40um x 130um, Pitch= 58um
 2. OLB Size= 15.5um x 100um, Pitch= 32um (every 3 bumps)
 3. Bump Height= 12±2um (Typ.)

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